

COMPAL CONFIDENTIAL

MODEL NAME : ADM60

PCB NO : DAA000AD000

BOM P/N : 4319XY31L01/L02

Park City 12" UMA

Skylake U

2015-09-25

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

X76@ : SATA REDRIVER OPTION

MB PCB

Part Number	Description
DAA000AD000	PCB 12K LA-C621P REV0 MB

Layout Dell logo



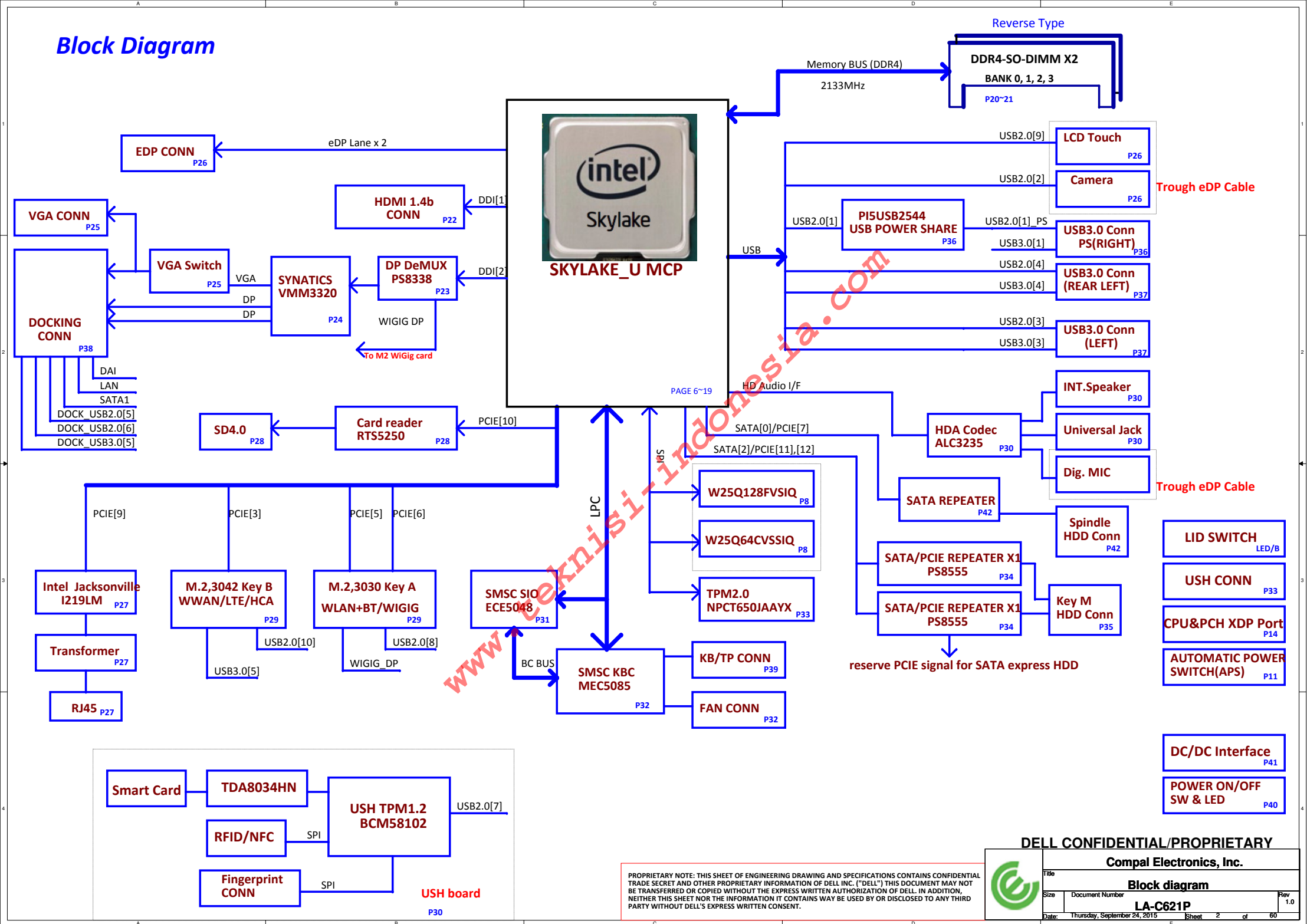
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REV: A00
PWB: 6N3K7

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Block Diagram



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Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

State	power plane				(M-OFF)	
		+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.5V_RUN	+3.3V_M 	+3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S0		ON	ON	ON	ON	ON
S3		ON	ON	OFF	ON	OFF
S5 S4/AC		ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist		OFF	OFF	OFF	OFF	OFF

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USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Right
USB3.0-2	SSIC-1			EDOCK PORT1
USB3.0-3	SSIC-2			JUSB1-->LEFT
USB3.0-4				JUSB2-->Rear LEFT
USB3.0-5		PCIE-1		M2 3042(WWAN)
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3042(HCA or QCA LTE)
		PCIE-4		NA
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	HDD SATA
		PCIE-8	SATA-1	EDOCK E-SATA
		PCIE-9		LOM
		PCIE-10		Card Reader
		PCIE-11	SATA-1*	M.2 Socket 3 (Key M) (PClex2 or SATA)
		PCIE-12	SATA-2	

16	PCie #12	SATA #2	X2
15	PCie #11	SATA #1*	X2
14	PCie #10	GbE	X4
13	PCie #9	GbE	X2
12	PCie #8	SATA #1	X2
11	PCie #7	SATA #0	X2
10	PCie #6		X4
9	PCie #5	GbE	X2
8	PCie #4	GbE	X2
7	PCie #3	GbE	X2
6	PCie #2		X4
5	PCie #1		X2
4	USB3 #4		
3	USB3 #3	SSIC #2	
2	USB3 #2	SSIC #1	
1	USB3 #1 (Capable of OTG)		

USB PORT#	DESTINATION
1	JUSB1-->Right
2	Camera
3	JUSB2-->LEFT
4	JUSB3-->Rear LEFT
5	EDOCK PORT1
6	EDOCK PORT2
7	USH
8	M.2 304230(BT)
9	Touch Screen
10	M2 3042(WWAN)

US\$	0	BIO
	1	NA

Check



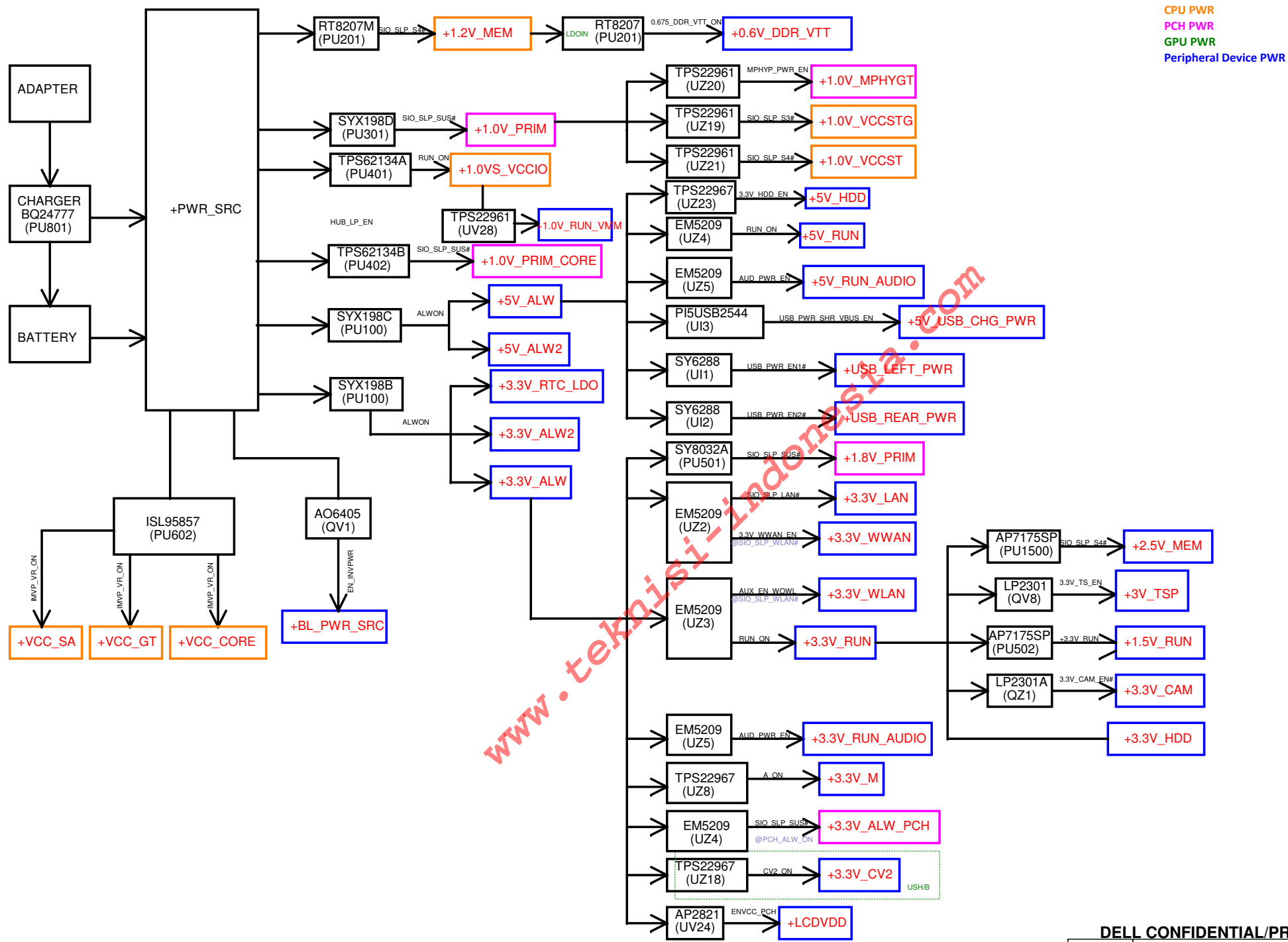
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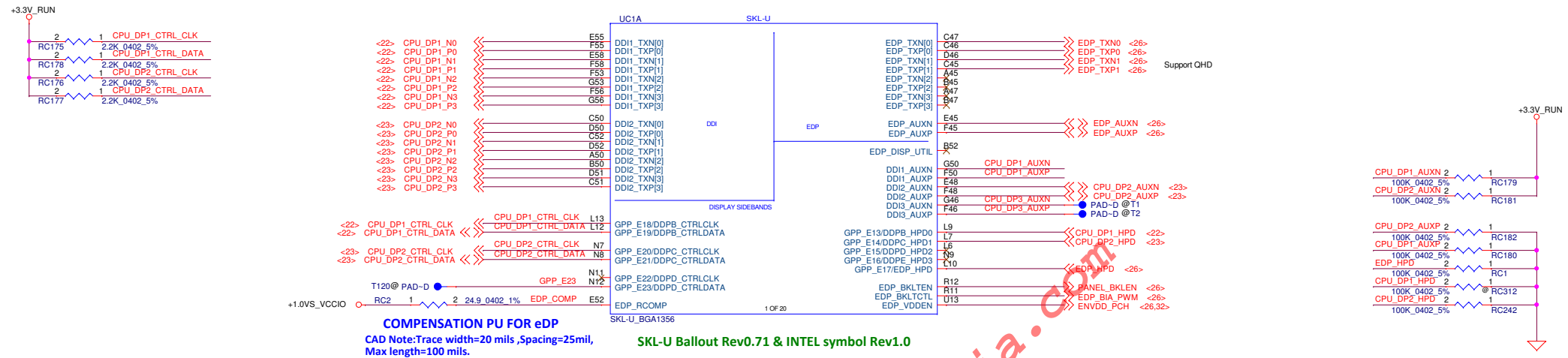


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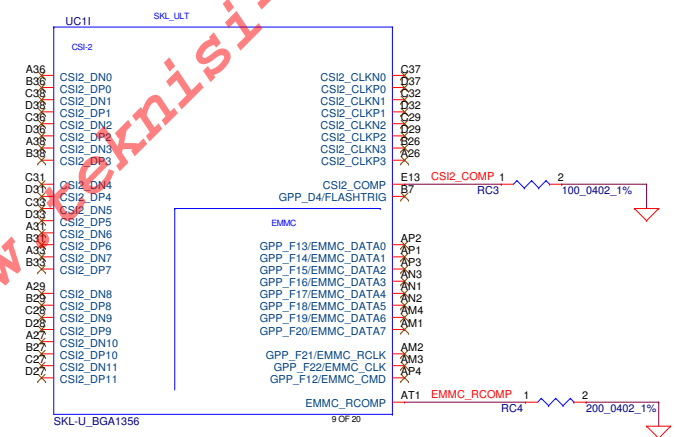


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CPU (1/14)

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DDR4, Ballout for side by side(Non-Interleave)

DDR4 COMPENSATION SIGNALS

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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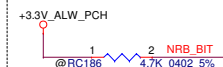
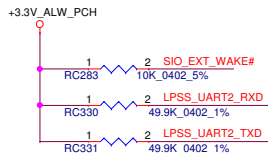
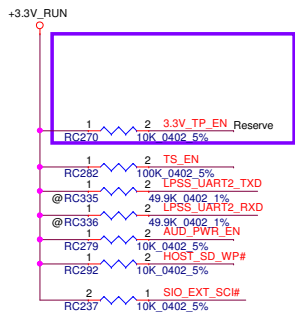
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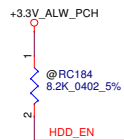
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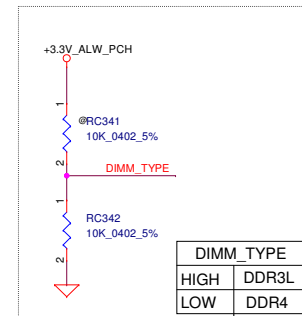
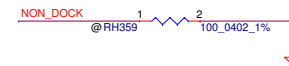
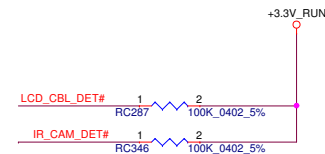
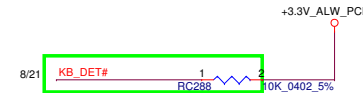
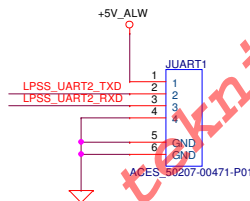
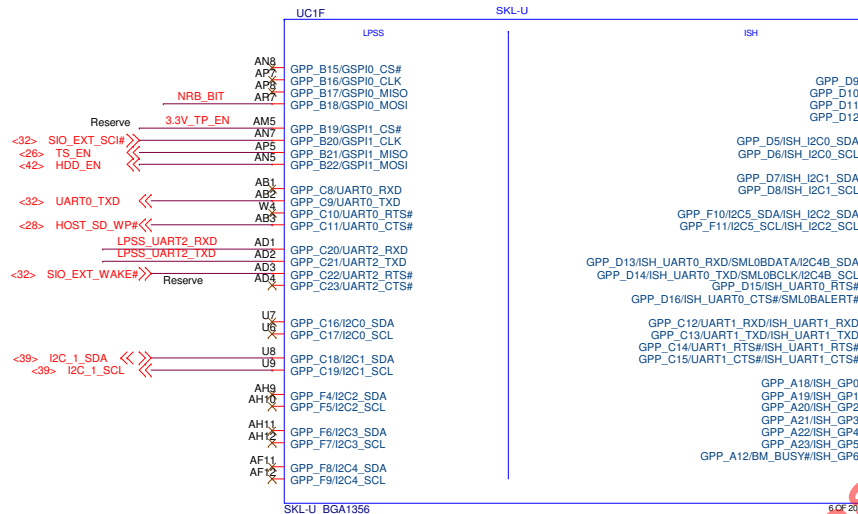
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NO REBOOT STRAP	
HIGH (DEFAULT)	No REBOOT
LOW (DEFAULT)	REBOOT ENABLE
Weak IPD	



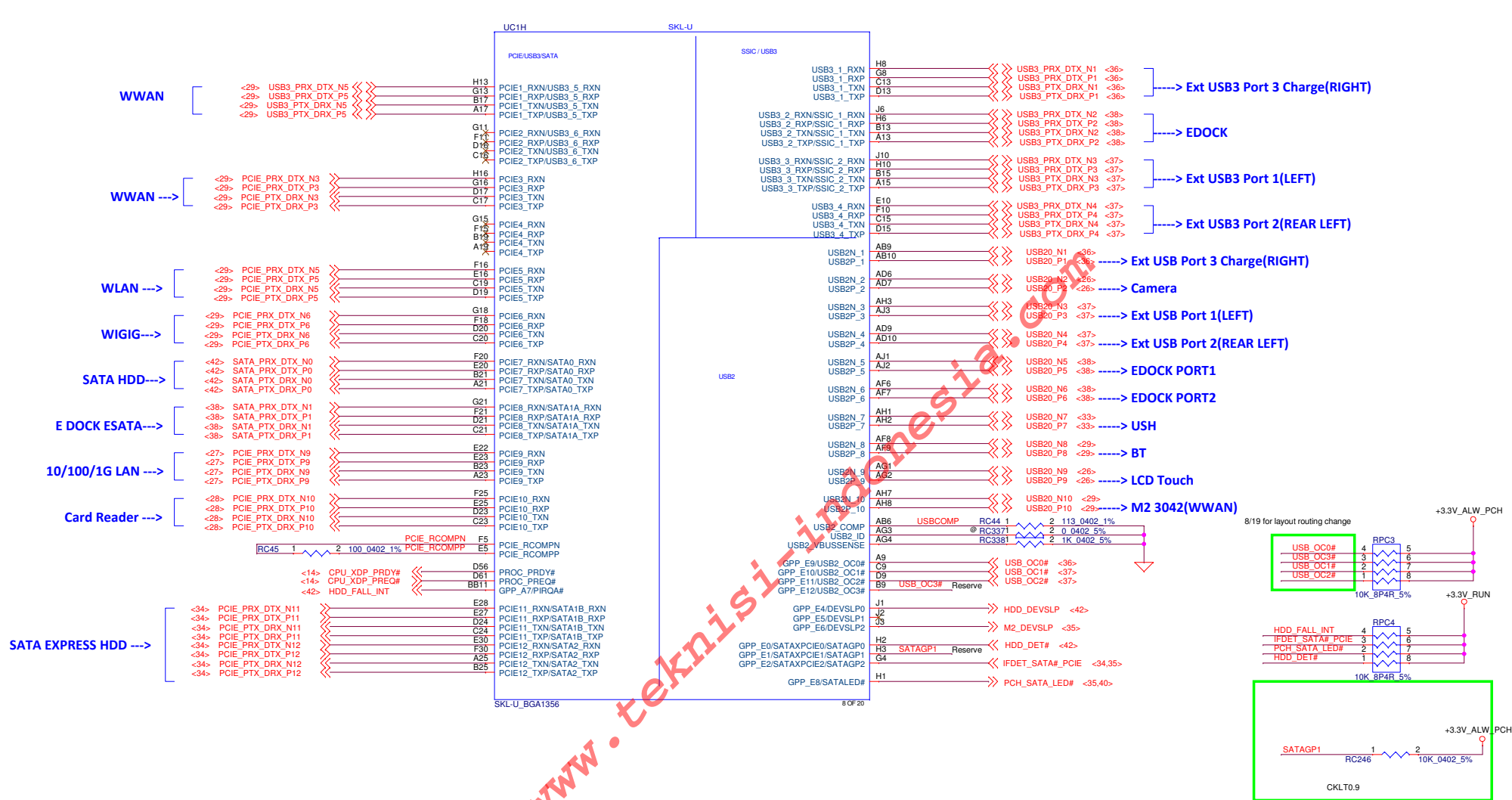
BOOT BIOS Destination(Bit 10)	
HIGH	LPC
LOW (DEFAULT)	SPI



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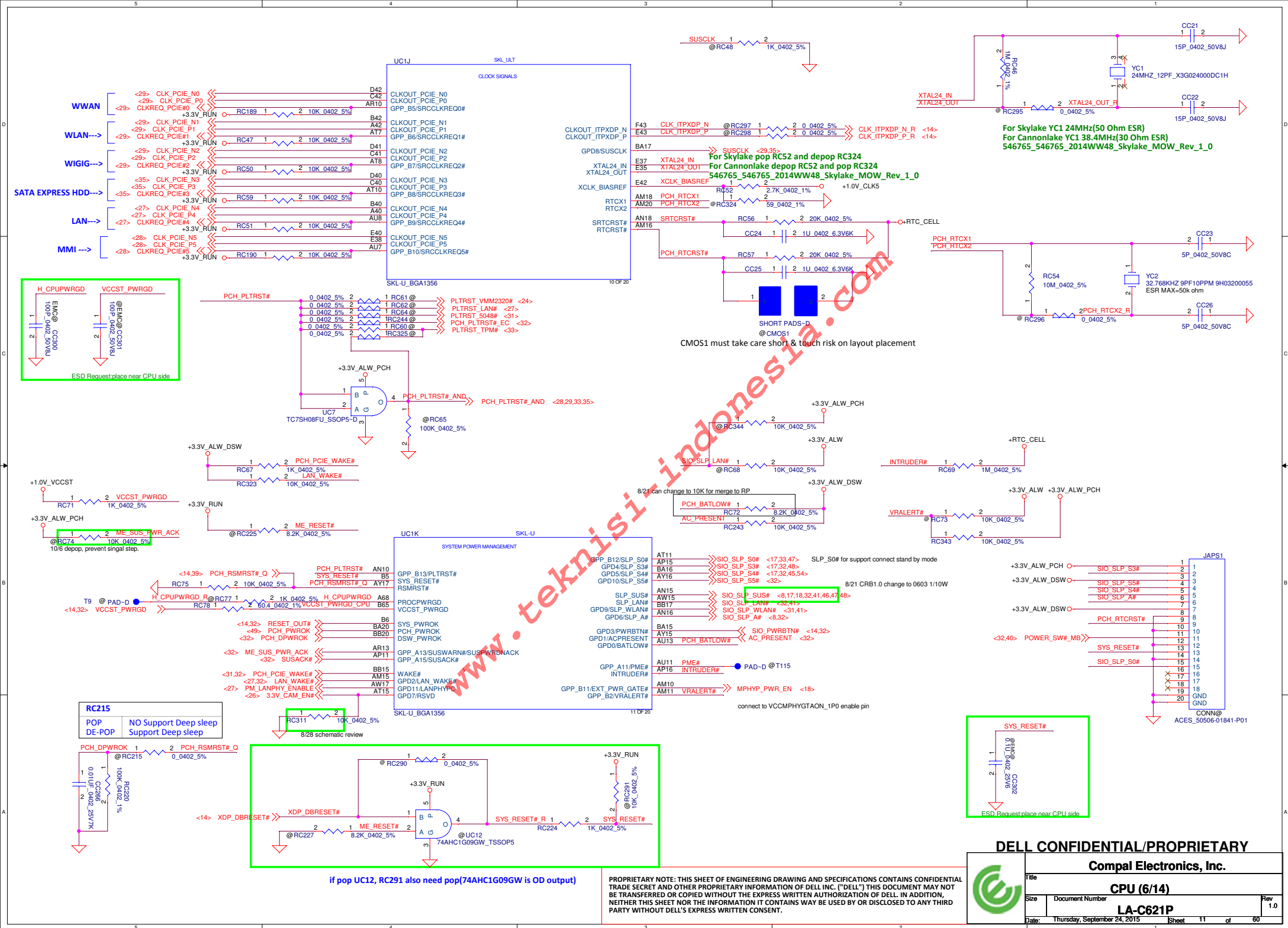
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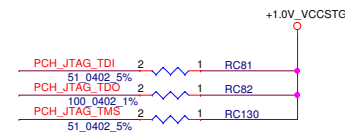
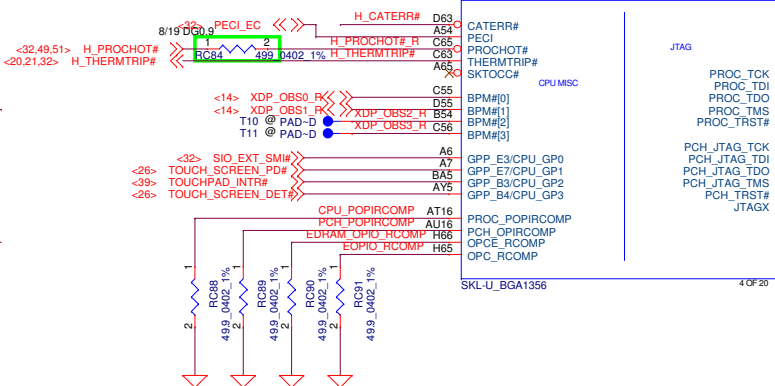
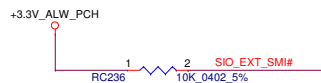
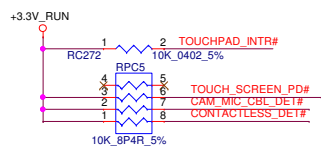
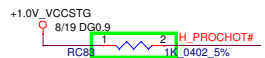
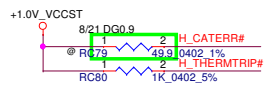
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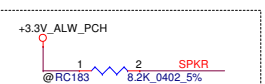
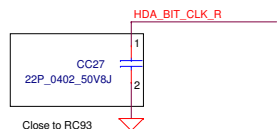
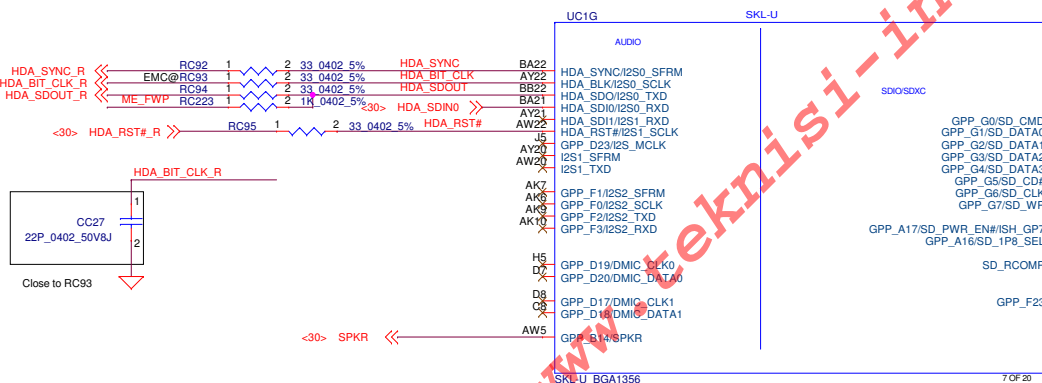
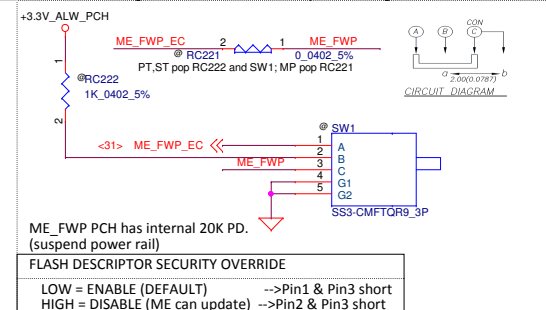
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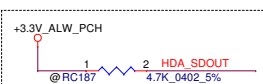




Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE



Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

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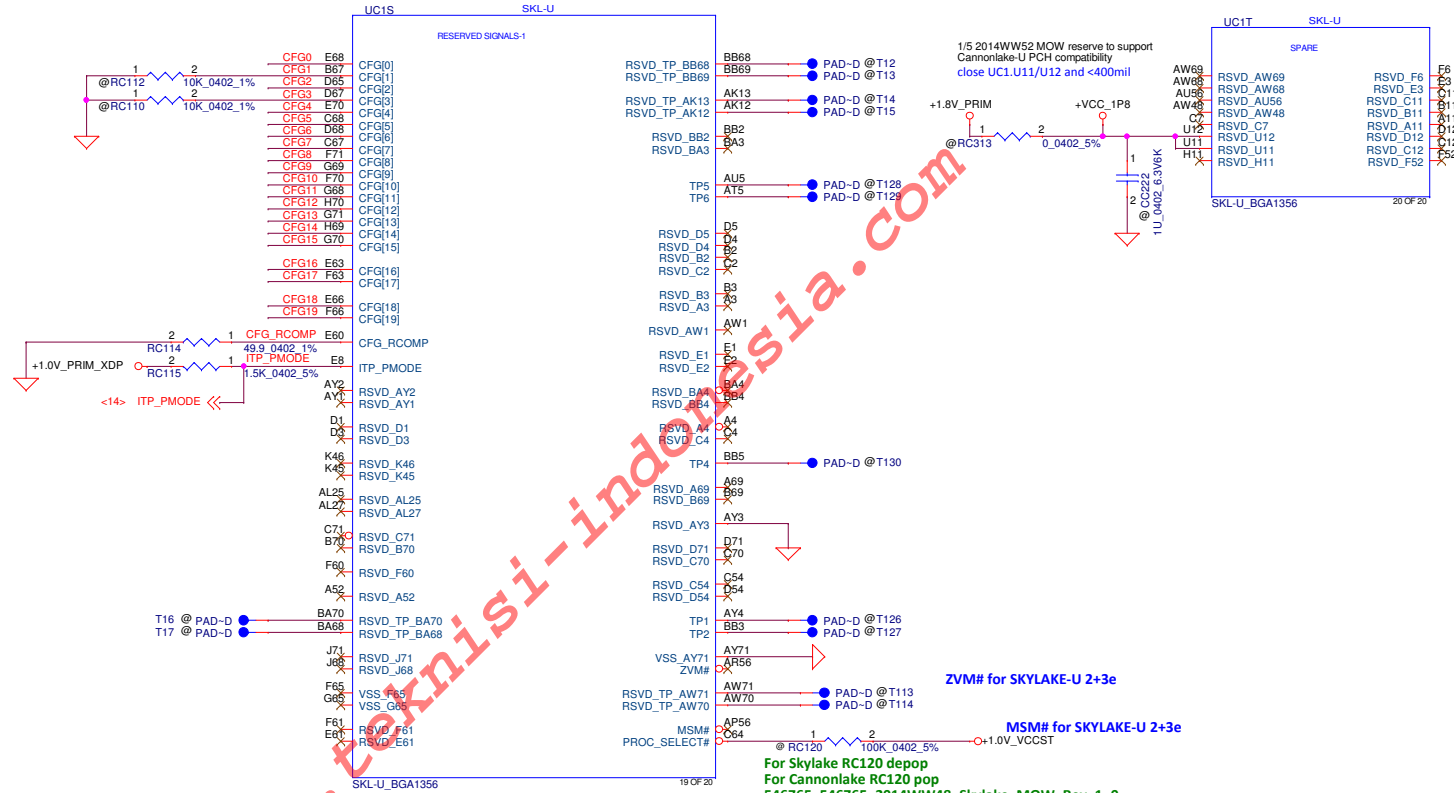
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Stall reset sequence	
HIGH(DEFAULT) LOW	No stall(Normal Operation) stall

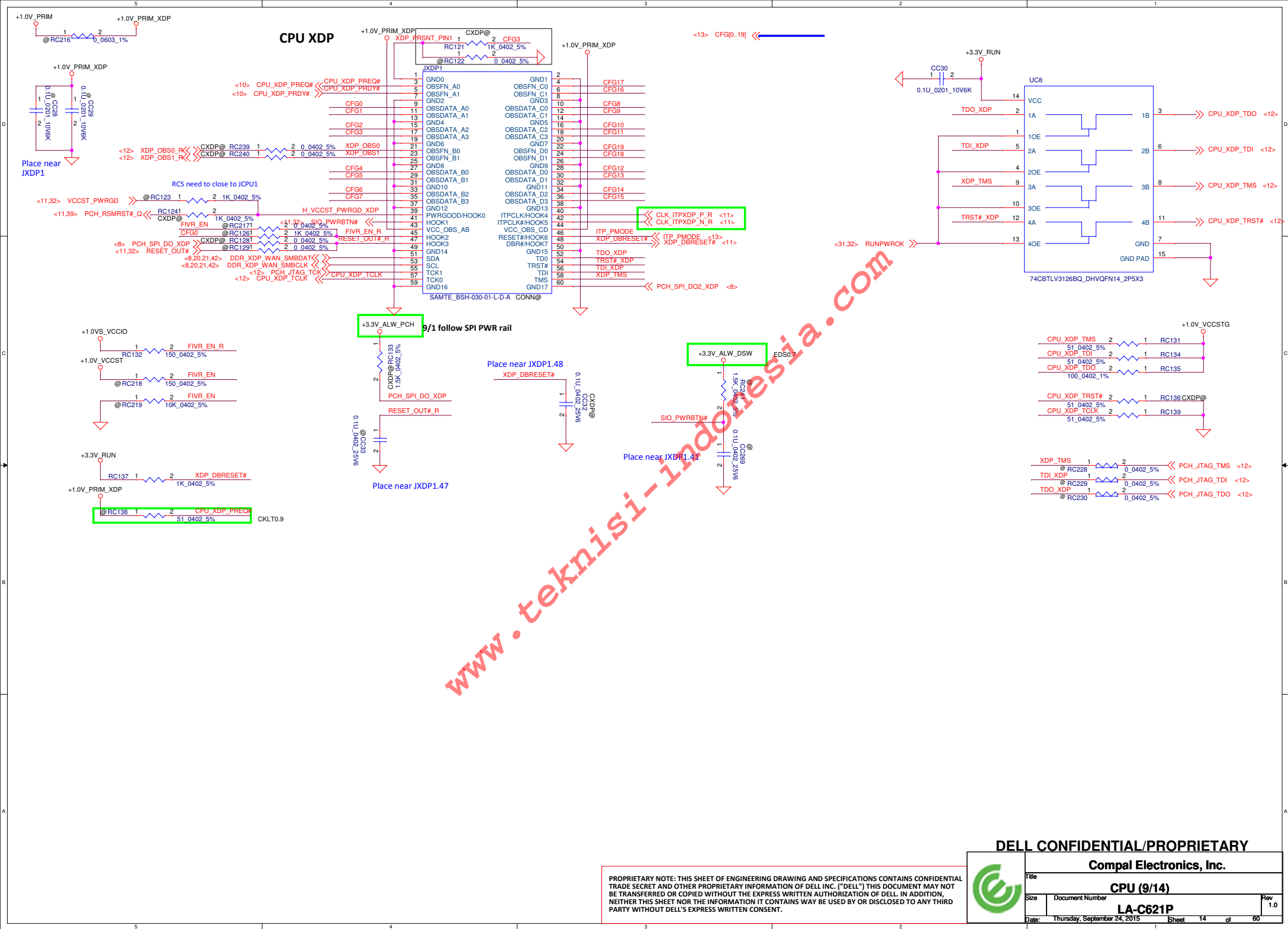
eDP enable	
HIGH(DEFAULT)	Disabled
LOW	Enabled

**CPU (8/14)**

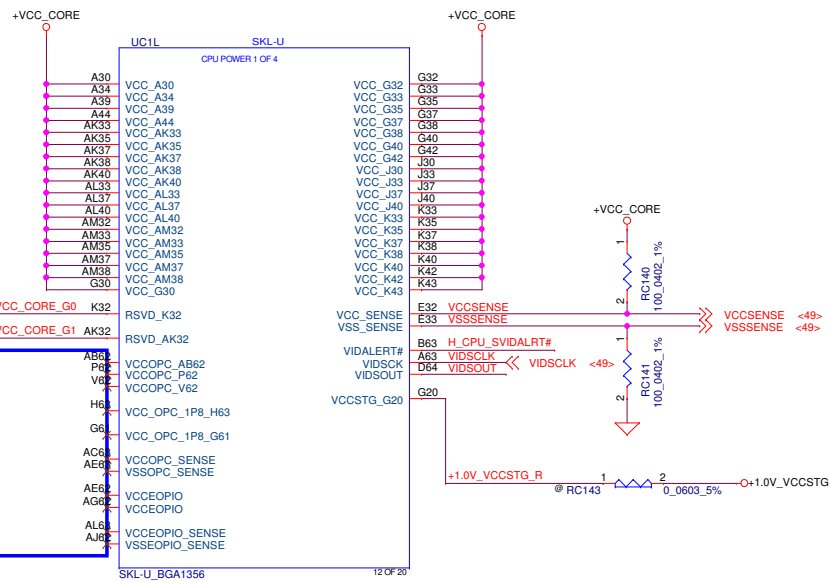
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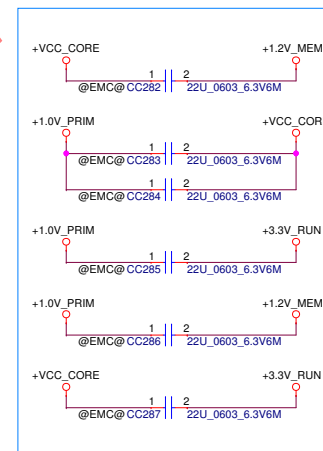
+VCC_CORE: 0.3~1.35V



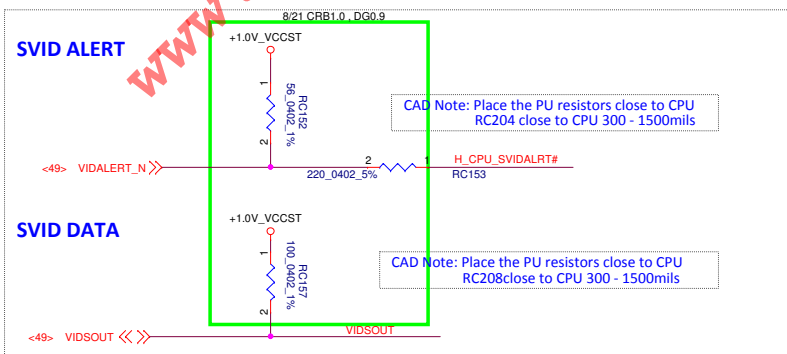
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Power source

ESD Request



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

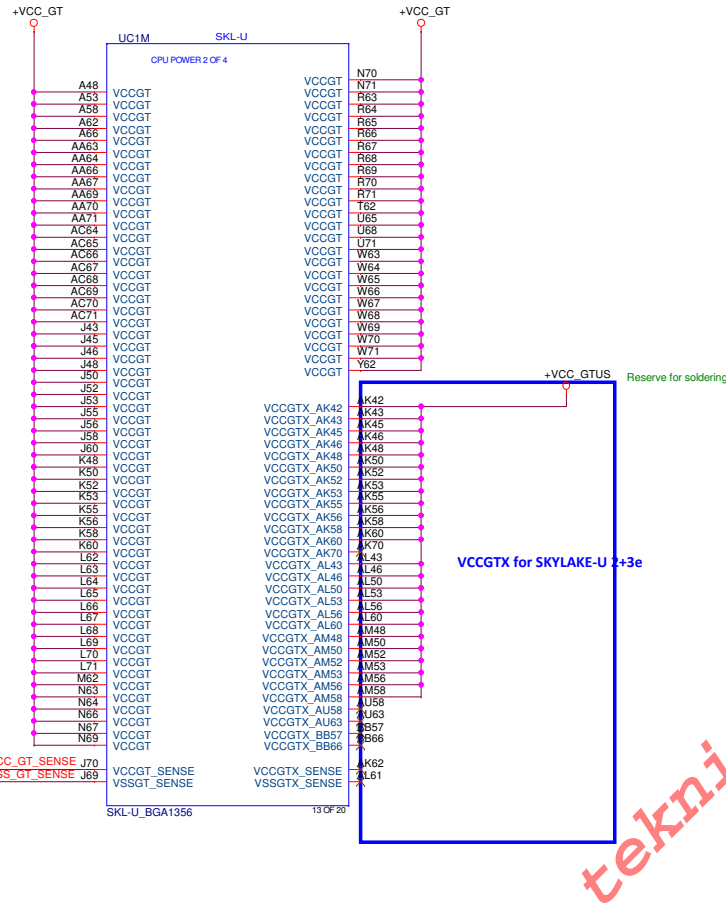


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+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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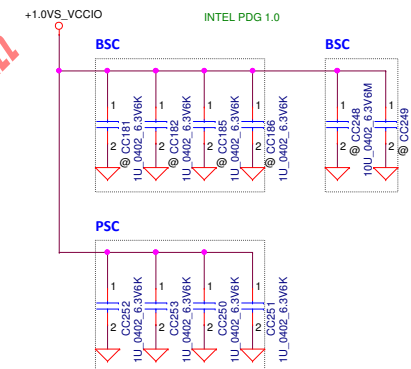
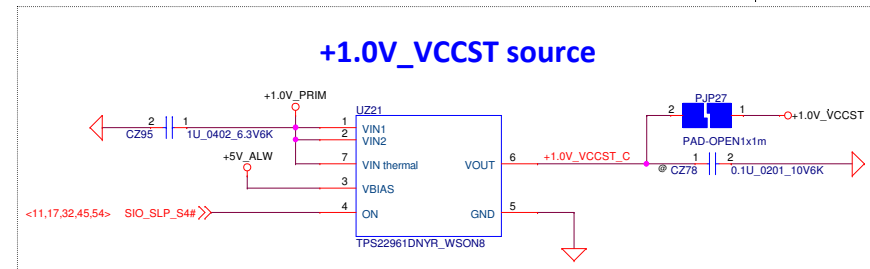
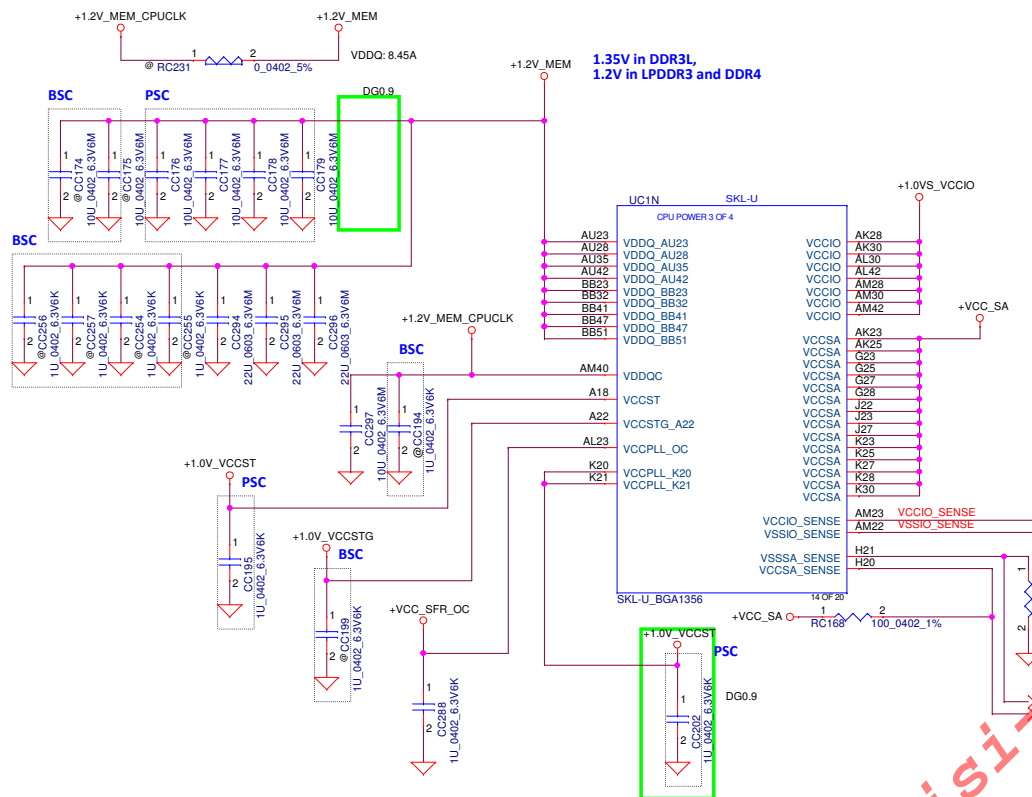
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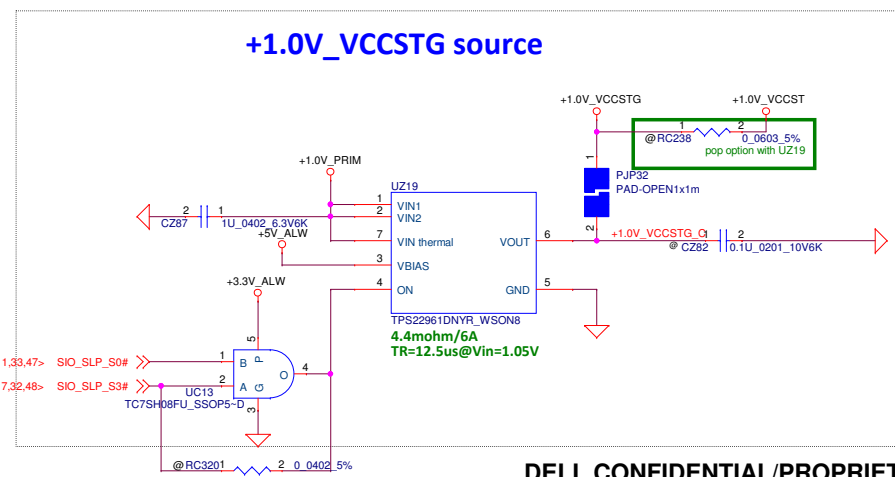
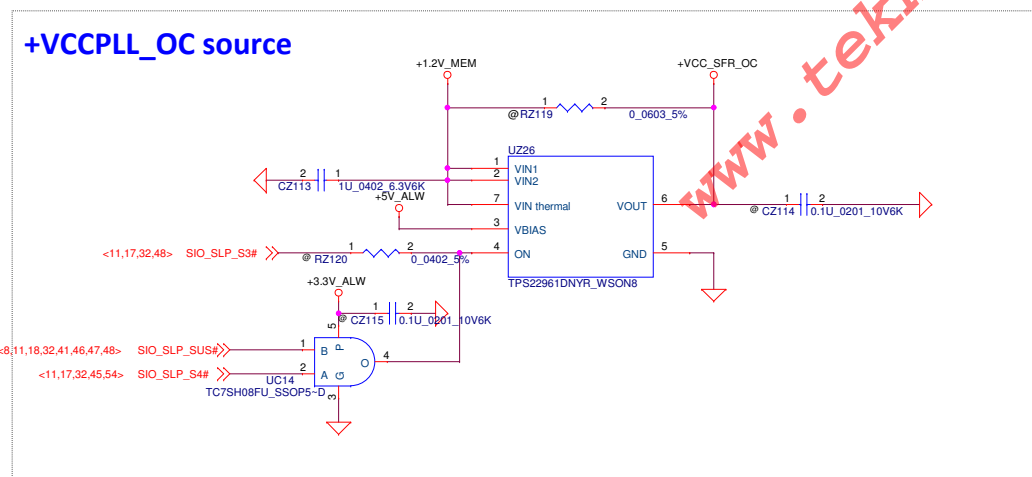


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	S0	S0ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW



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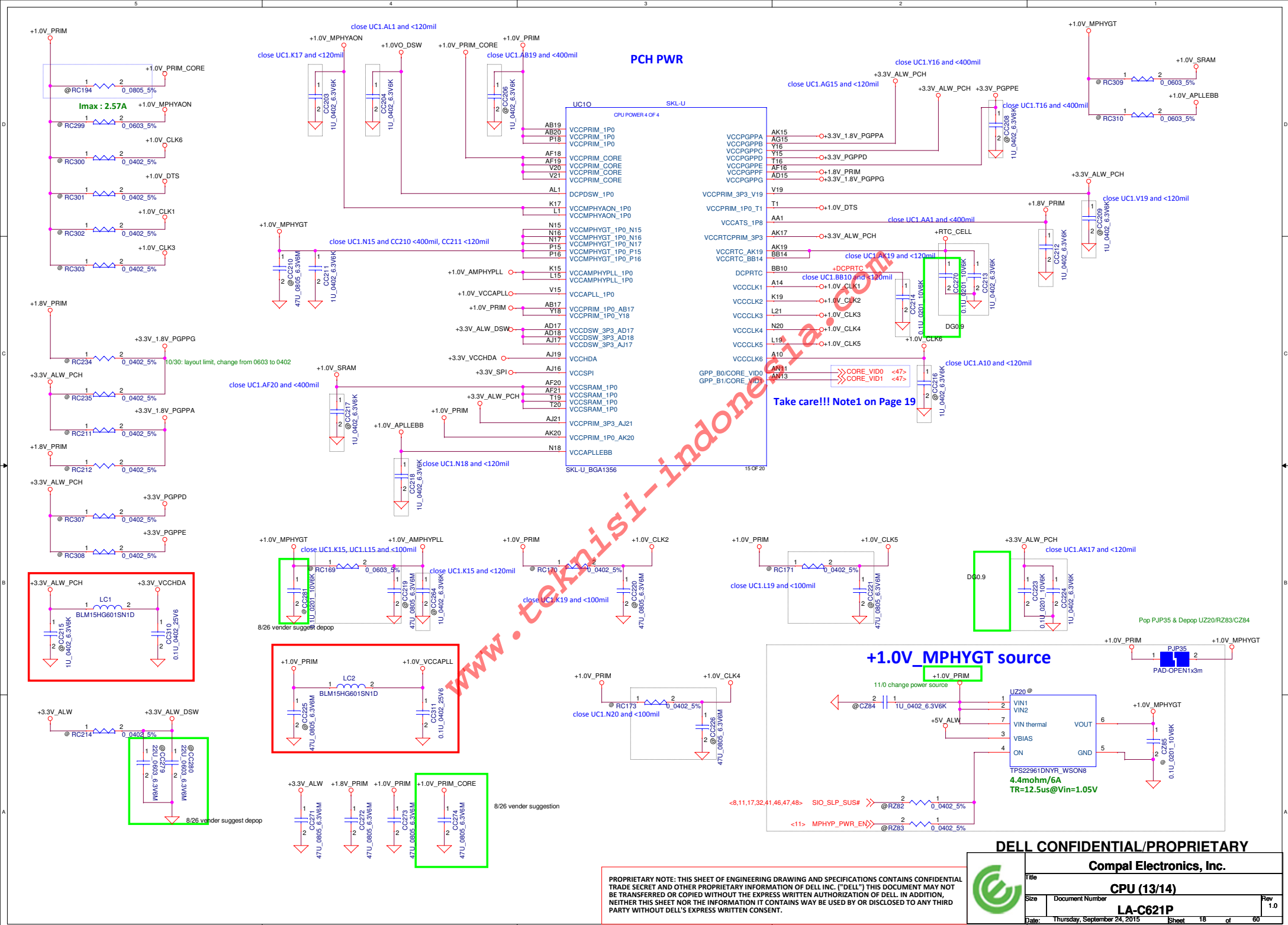
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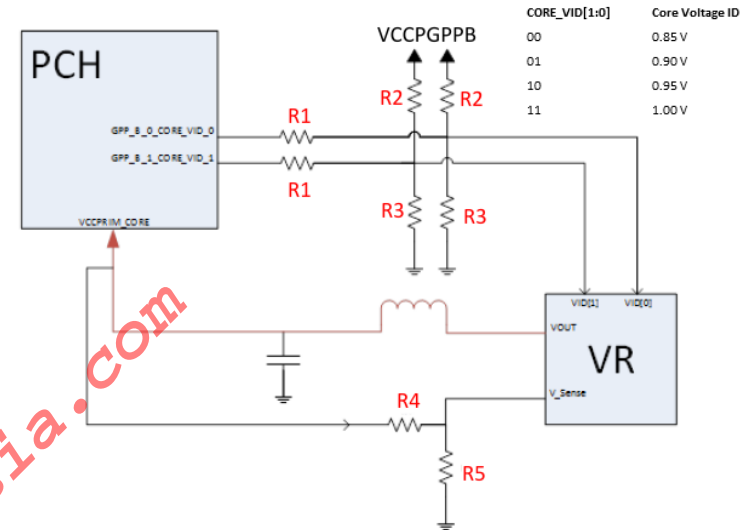
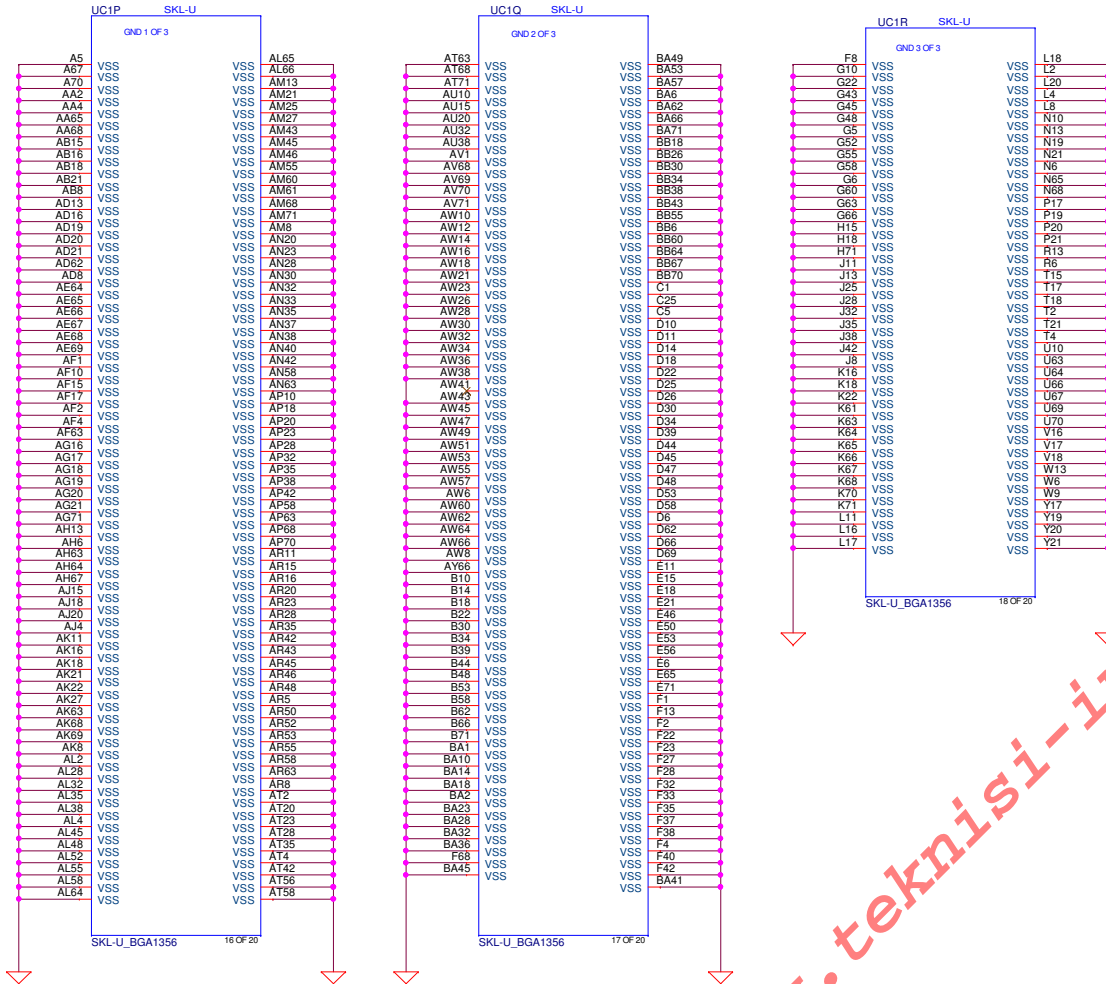
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Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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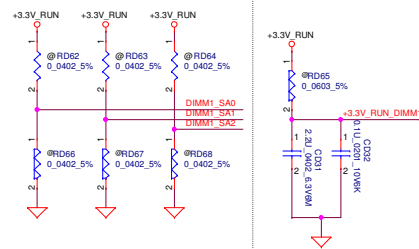
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+12V MEM			DDR#1			+12V MEM		
DDR A_D1	1	VSS1	2	VSS2	2	DDR A_D4		
DDR A_D0	3	DQ1	4	DQ4	6	DDR A_D5		
DDR A_D0S0	7	VSS5	8	VSS4	10			
DDR A_D0S1	11	VSS5	12	VSS8	12			
DDR A_D6	13	DQ0-0	14	DQ0-0	16			
DDR A_D6	17	DQ0-0	18	DQ6-18	20	DDR A_D3		
DDR A_D2	21	VSS10	22	VSS11	24	DDR A_D9		
DDR A_D13	23	VSS12	24	DQ12	26			
DDR A_D13	27	DQ13	28	VSS13	30			
DDR A_D12	29	VSS14	30	DQ8	32	DDR A_D8		
	31	DQ9	32	VSS15	34	DDR A_D0S#1		
	33	DQ81	34	DQ81	36	DDR A_D0S#1		
DDR A_D15	35	DM1_nDBI_n	36	VSS18	38	DDR A_D10		
	37	DQ14	38	DQ14	40			
DDR A_D14	41	VSS19	42	VSS20	44	DDR A_D11		
DDR A_D35	43	VSS21	44	VSS22	46	DDR A_D32		
DDR A_D37	45	DQ21	46	DQ20	48			
DDR A_D37	49	VSS24	50	VSS24	52	DDR A_D36		
DDR A_D0S#4	51	DQ16	52	DQ16	54			
DDR A_D0S#4	53	VSS25	54	DM2_nDBI2_n	56			
DDR A_D38	55	DQ52	56	VSS27	58	DDR A_D39		
DDR A_D38	59	DQ52	60	DQ22	62	DDR A_D33		
DDR A_D34	61	DQ23	62	VSS29	64	DDR A_D40		
DDR A_D44	63	VSS30	64	DQ18	66			
DDR A_D44	65	DQ19	66	VSS31	68			
DDR A_D44	67	VSS32	68	DQ28	70	DDR A_D41		
DDR A_D46	69	DQ9	70	VSS33	72			
DDR A_D46	71	VSS34	72	DQ24	74	DDR A_D0S#5		
DDR A_D42	73	DQ25	74	VSS35	76	DDR A_D0S#5		
DDR A_D42	75	VSS36	76	DQ3	78	DDR A_D47		
DDR A_D46	77	DM2_nDBI3_n	78	DQ33	80			
	79	VSS37	80	DQ31	82	DDR A_D47		
DDR A_D46	81	VSS39	82	VSS40	84			
	83	DQ6	84	DQ27	86			

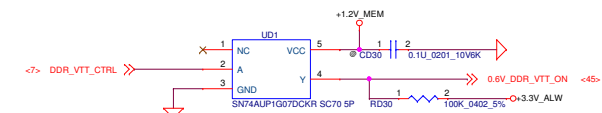
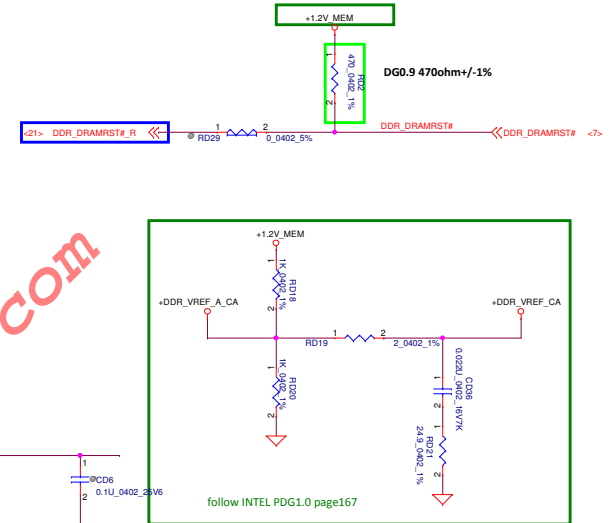
Figure 10 shows the pin connections for the 12V MEM module. The diagram illustrates two identical modules connected to a 12V MEM supply. Each module has a 12V MEM input, a GND connection, and a series of output pins labeled C1B5, C1B4, C1B3, C1B2, C1B1, C1B0, C1A5, C1A4, C1A3, C1A2, C1A1, C1A0, C1B5, C1B4, C1B3, C1B2, C1B1, C1B0, C1A5, C1A4, C1A3, C1A2, C1A1, C1A0. The outputs are connected to a 12V MEM supply and a GND connection. The diagram is labeled "© C2021 TDK" and "3201_001_701 - RM".

[illegible]

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

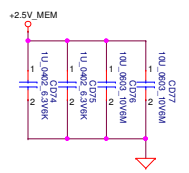
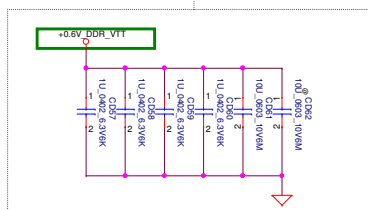
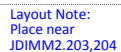
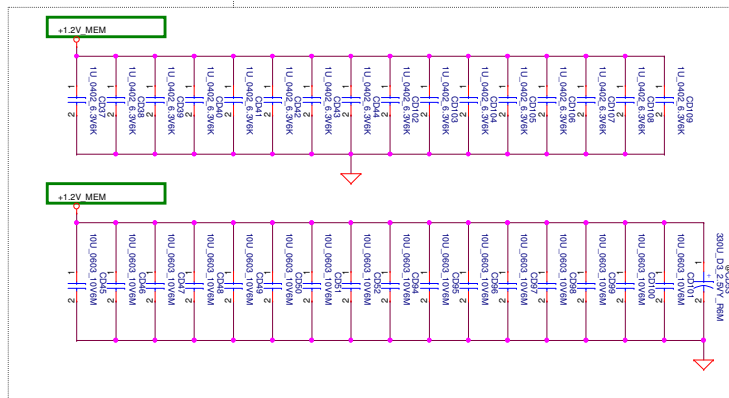


<8,14,21,42> DDR_XDP_WAN_SMBCLK <<>> +3.3V_RUN_DIMM1 253 VSS93 254 SDA 255 SCL 256 DIMM1_SA0 <<>> DDR_XDP_WAN_SMBDAT <8,14,21,42>

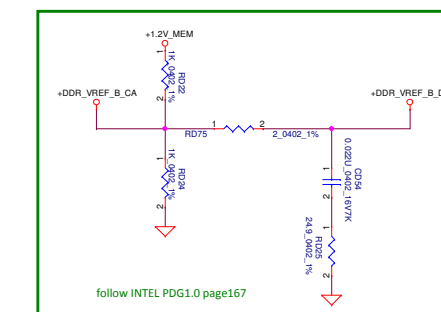
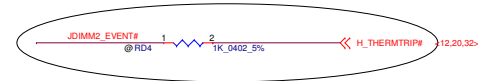
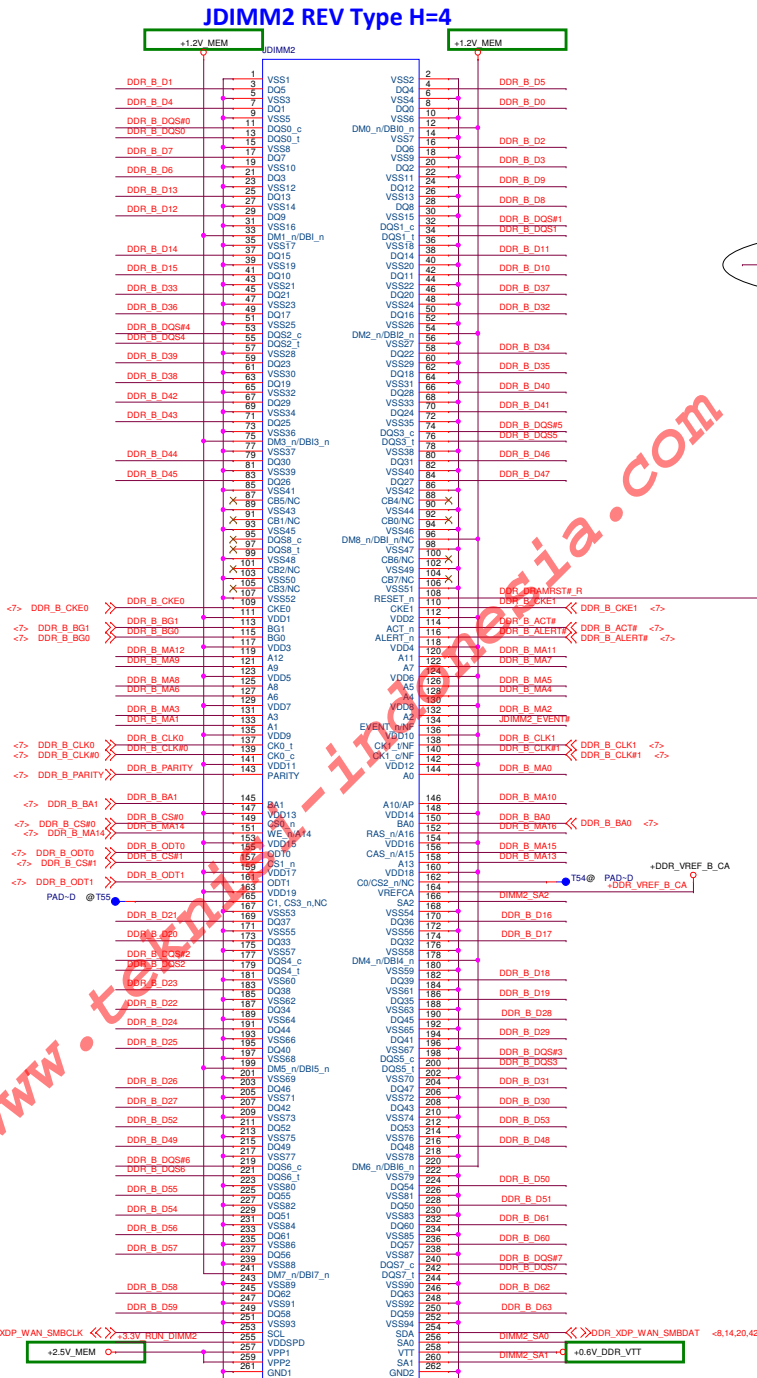
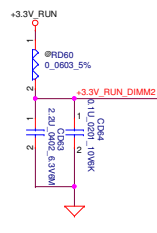
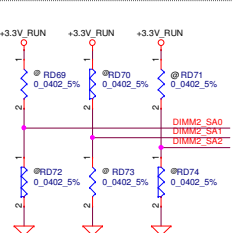


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DDR4			
Size	Document Number		Rev
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	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0



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DDR4

LA-C621P

Rev

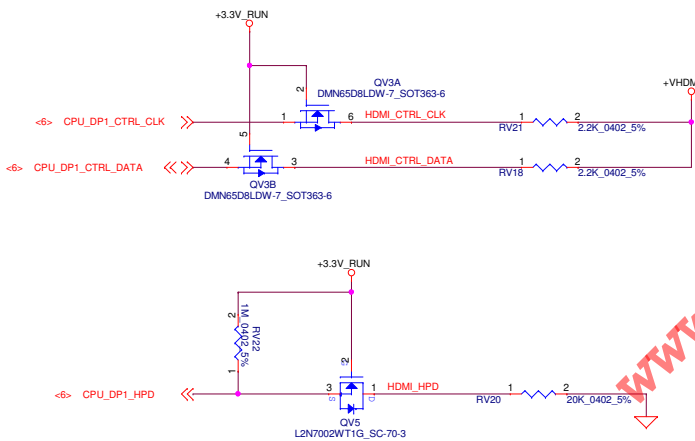
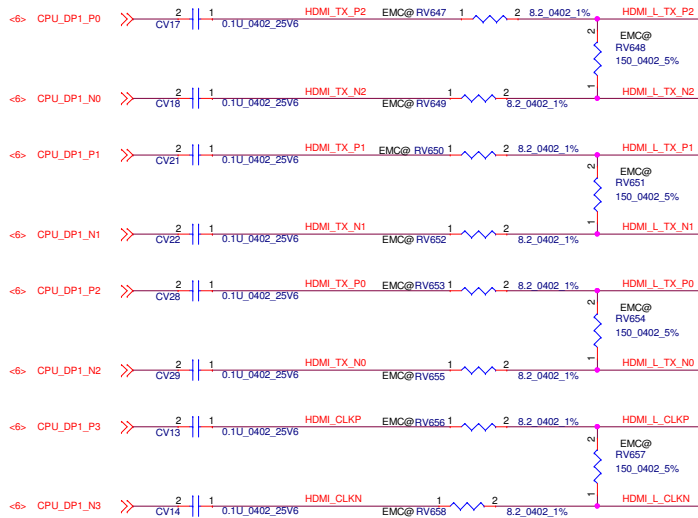
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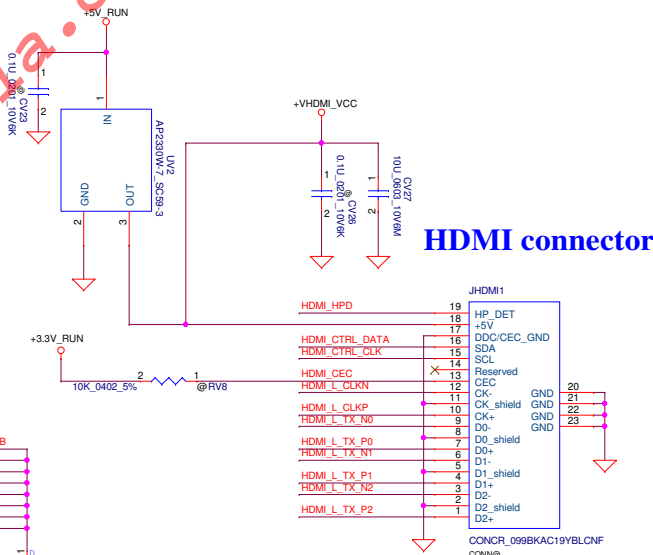
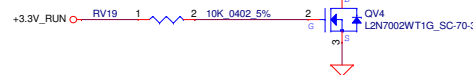
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HDMI TX P2	RV10	1	2	470	0402	1%	HDMI_OB
HDMI TX N2	RV11	1	2	470	0402	1%	
HDMI TX P1	RV12	1	2	470	0402	1%	
HDMI TX N1	RV13	1	2	470	0402	1%	
HDMI TX P0	RV14	1	2	470	0402	1%	
HDMI TX N0	RV15	1	2	470	0402	1%	
HDMI_CLKP	RV16	1	2	470	0402	1%	
HDMI_CLKN	RV17	1	2	470	0402	1%	



HDMI connector

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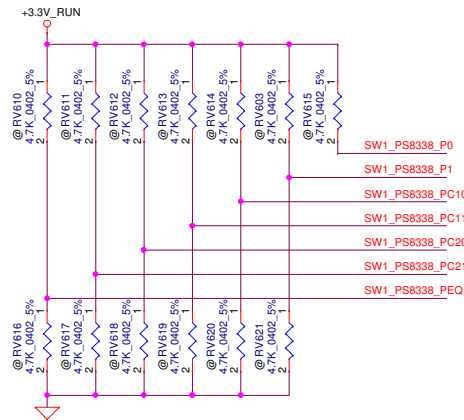
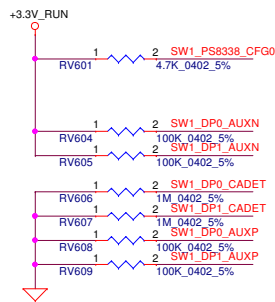
HDMI CONN

LA-C621P

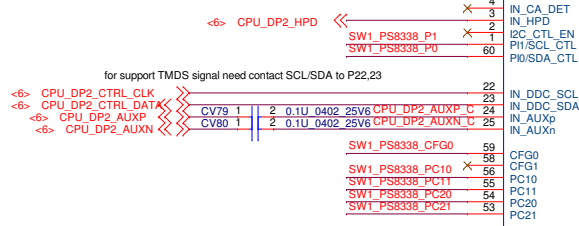
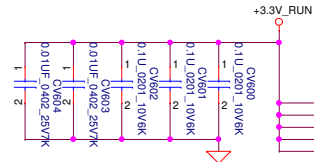
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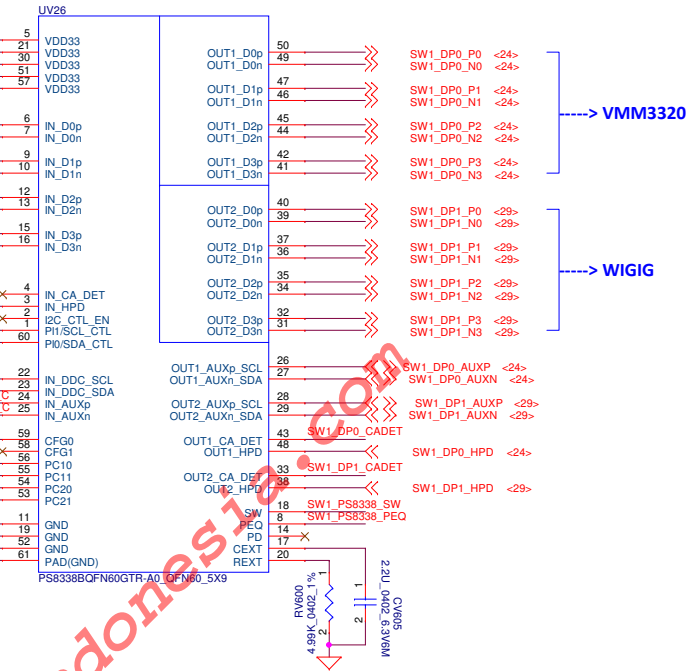
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- <6> CPU_DP2_N0
- <6> CPU_DP2_P1
- <6> CPU_DP2_N1
- <6> CPU_DP2_P2
- <6> CPU_DP2_N2
- <6> CPU_DP2_P3
- <6> CPU_DP2_N3



Dock has high priority when both ports plugged



<25,27,31> DOCKED

Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O

For Control Switching Mode (CFG0 = L):
 SW = L: Port1 is selected (default)
 SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H):
 SW = L: Port1 has higher priority when both ports are plugged (default)
 SW = H: Port2 has higher priority when both ports are plugged

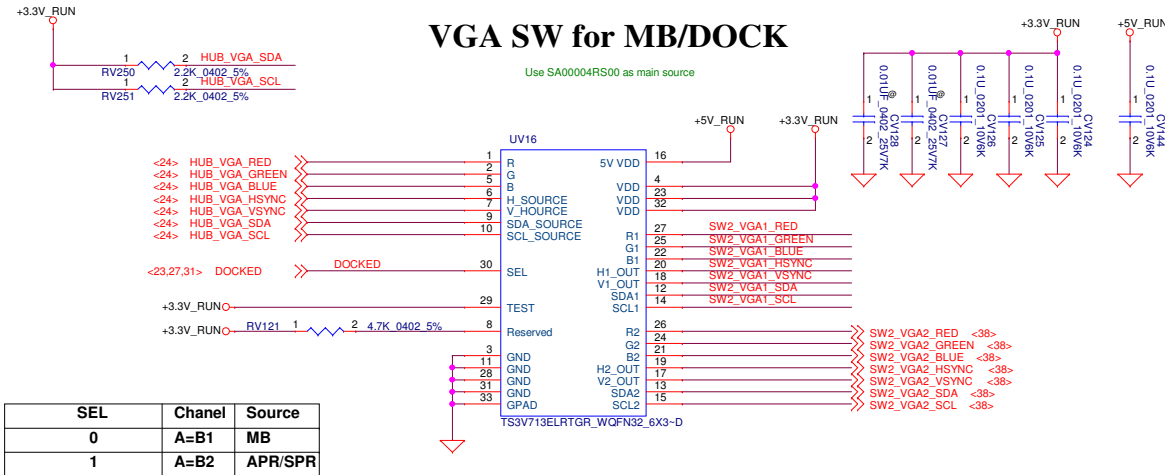
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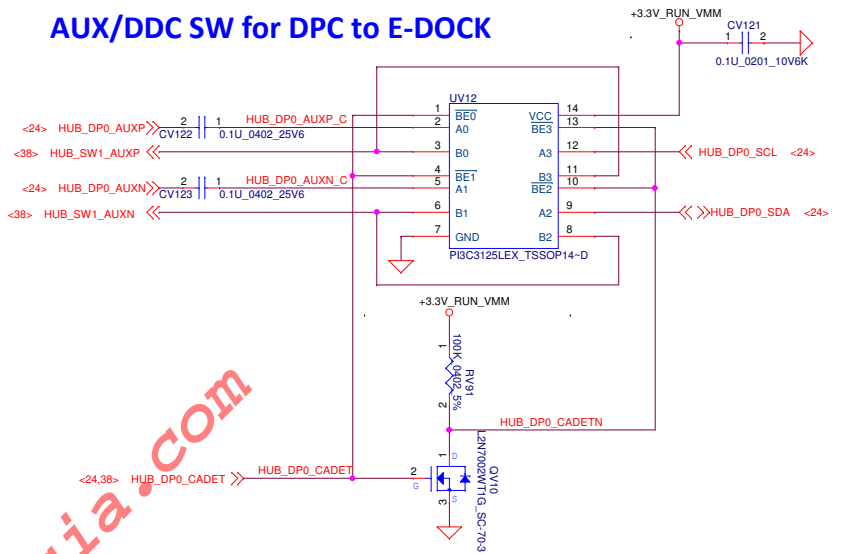
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VGA SW for MB/DOCK

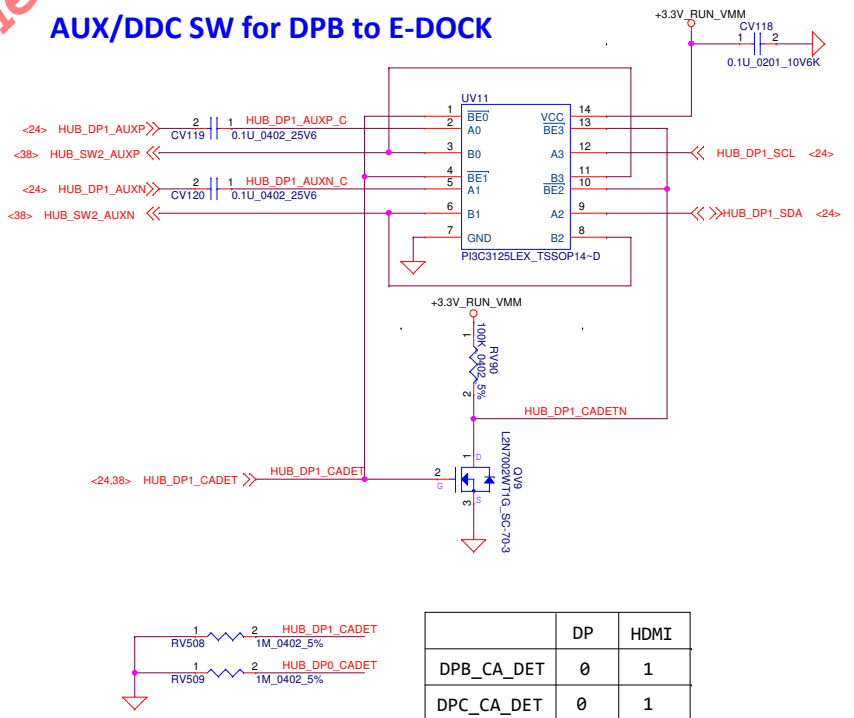
Use SA00004RS00 as main source



AUX/DDC SW for DPC to E-DOCK



AUX/DDC SW for DPB to E-DOCK



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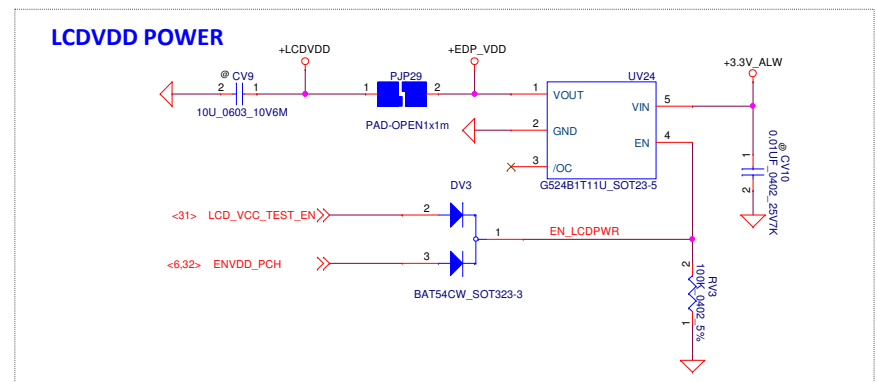
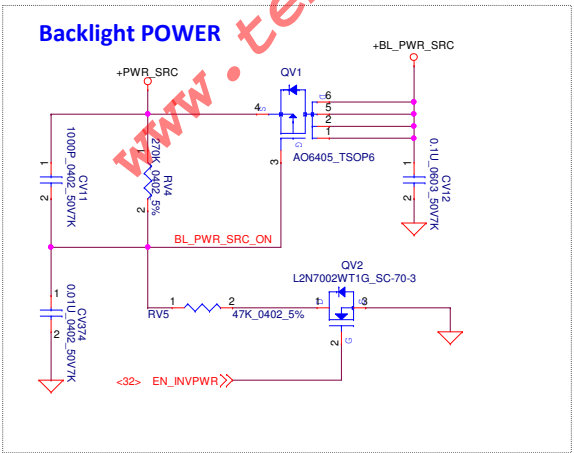
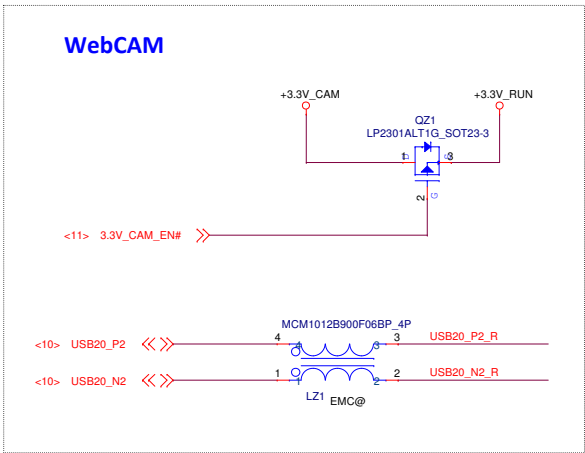
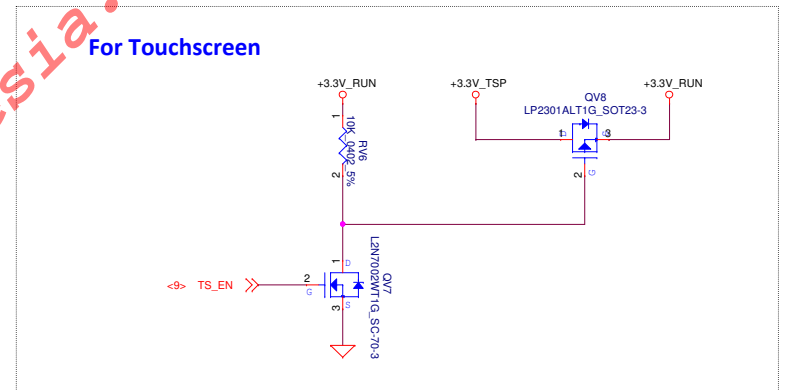
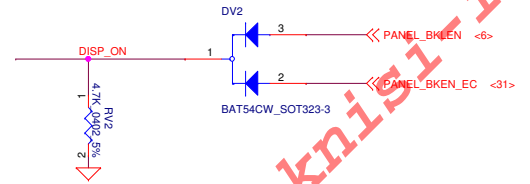
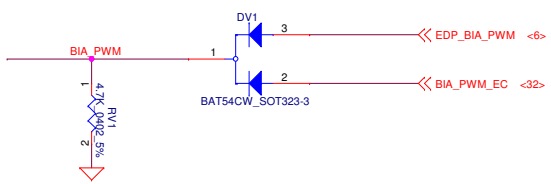
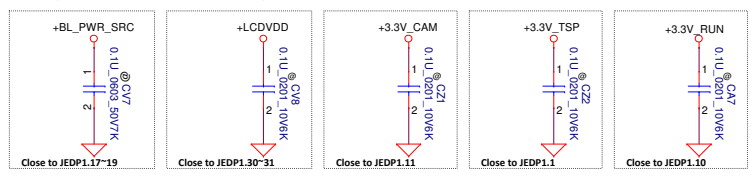
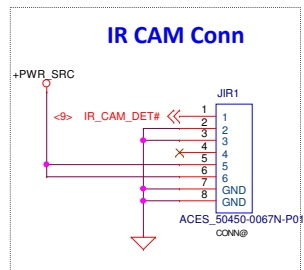
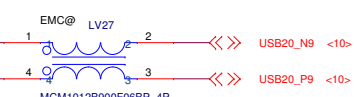
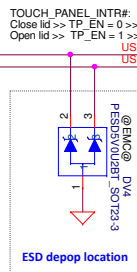
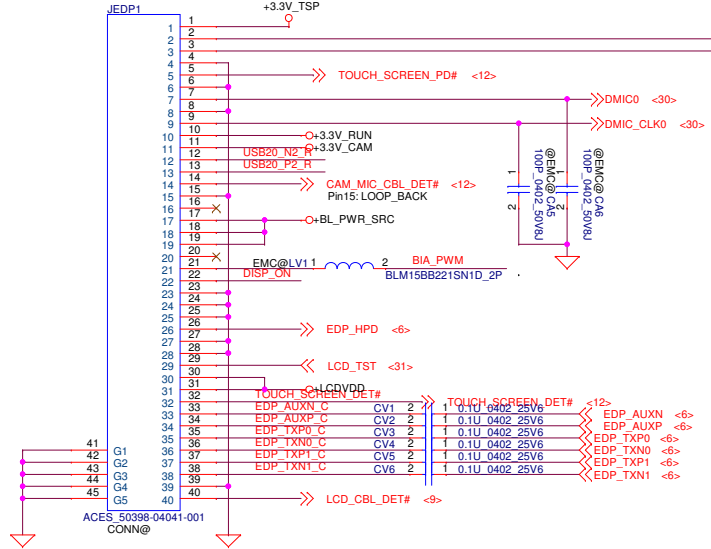
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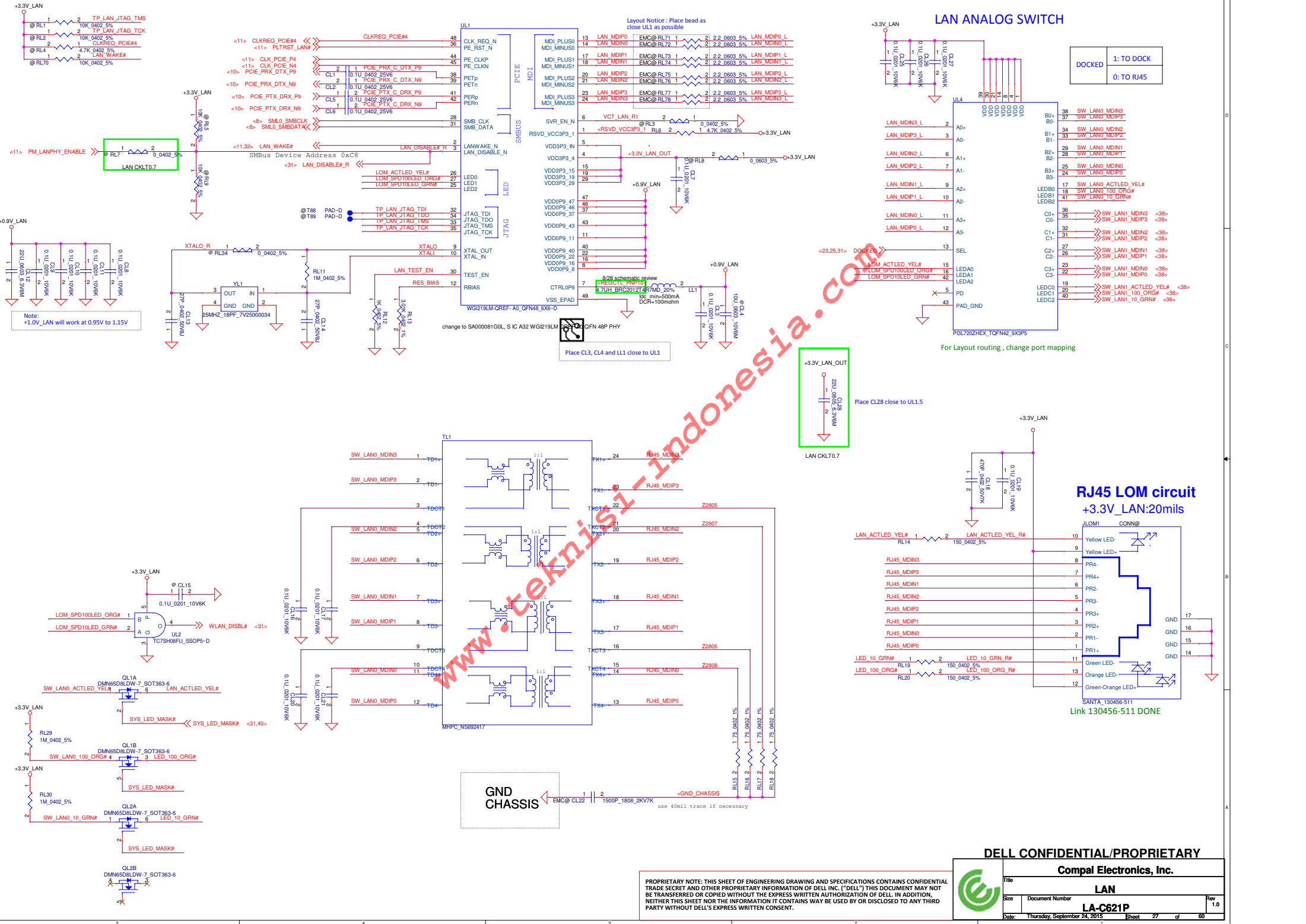
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eDP CONN & Touch screen

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LAN ANALOG SWITCH

DOCKED	1: TO DOCK
	0: TO RJ45

For Layout routing, change port mapping

RJ45 LOM circuit
+3.3V_LAN:20mils

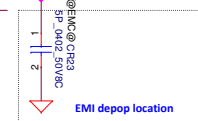
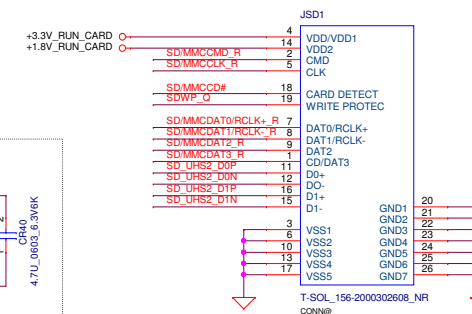
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Title LAN		
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7/18 Vender suggest.

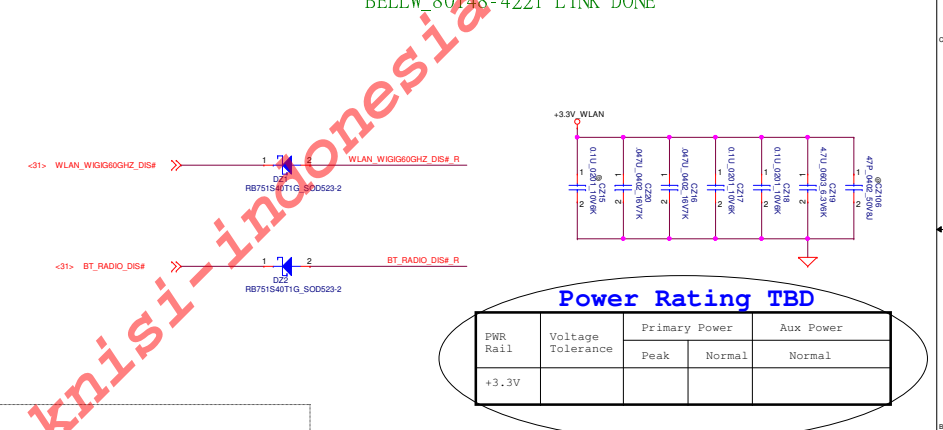
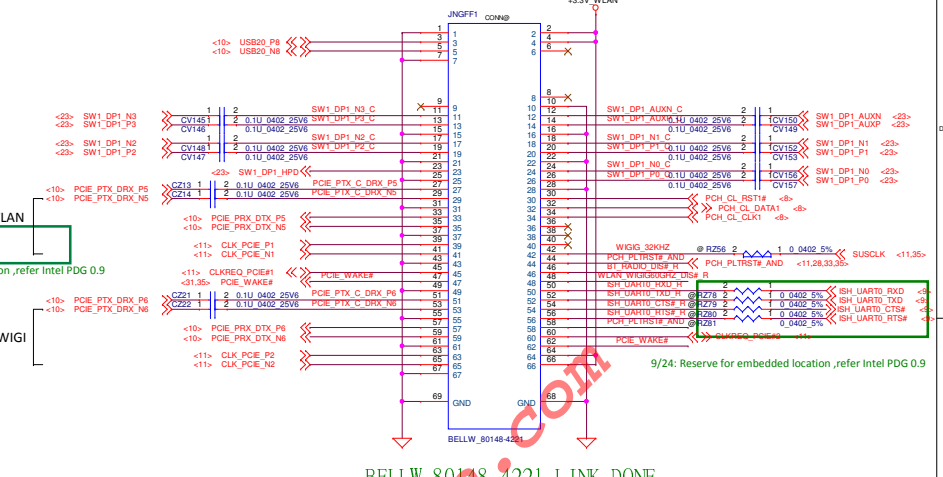
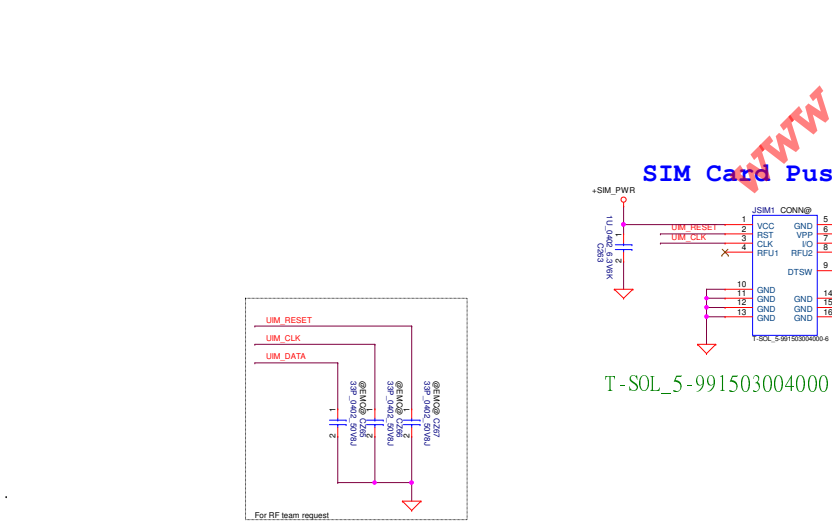
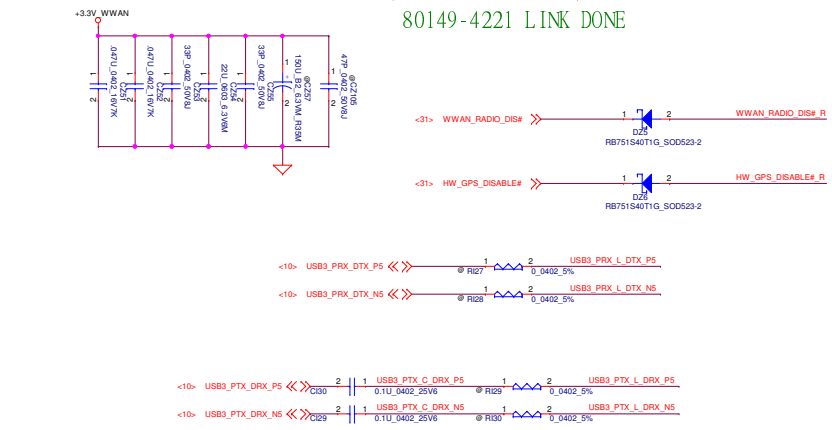
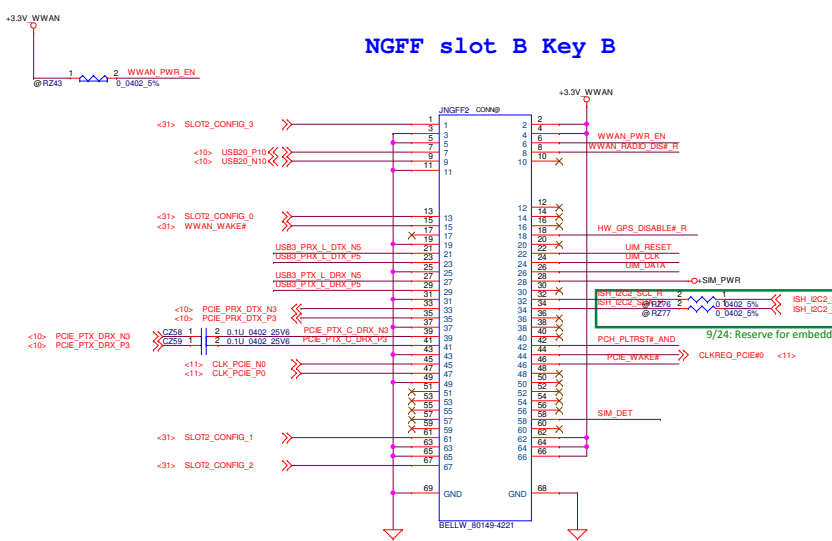
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Power Rating TBD				
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

[illegible]

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Internal Speakers Header

[illegible][illegible]

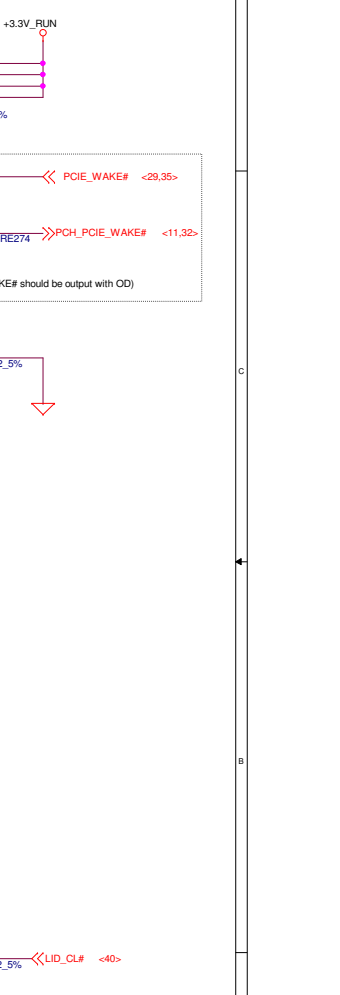
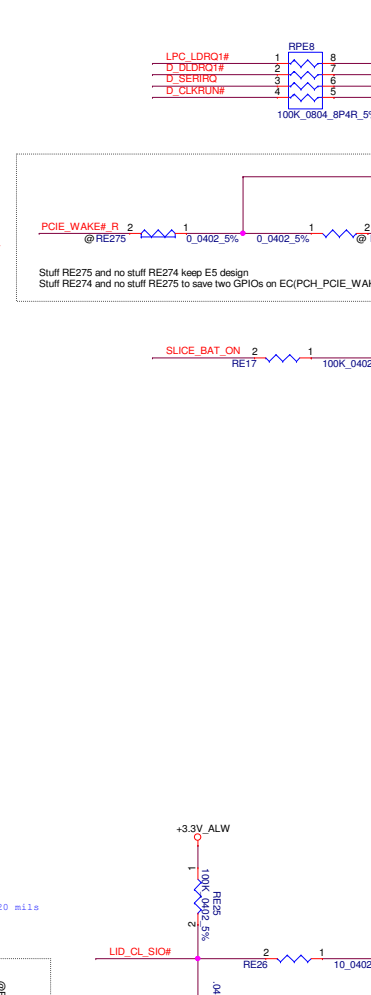
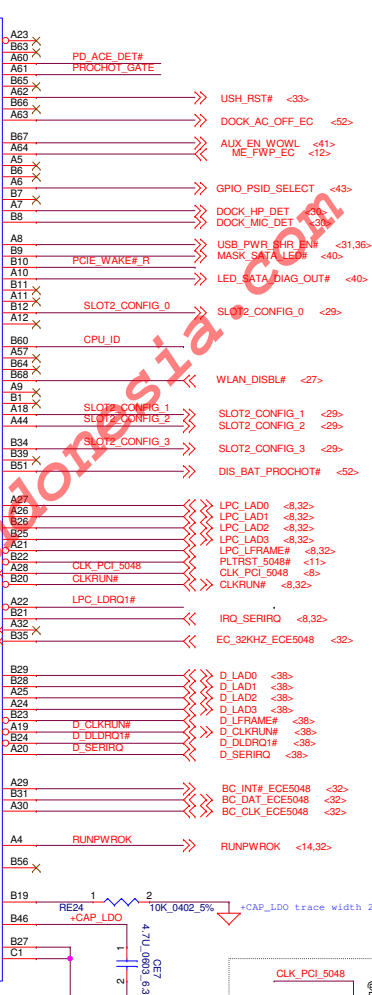
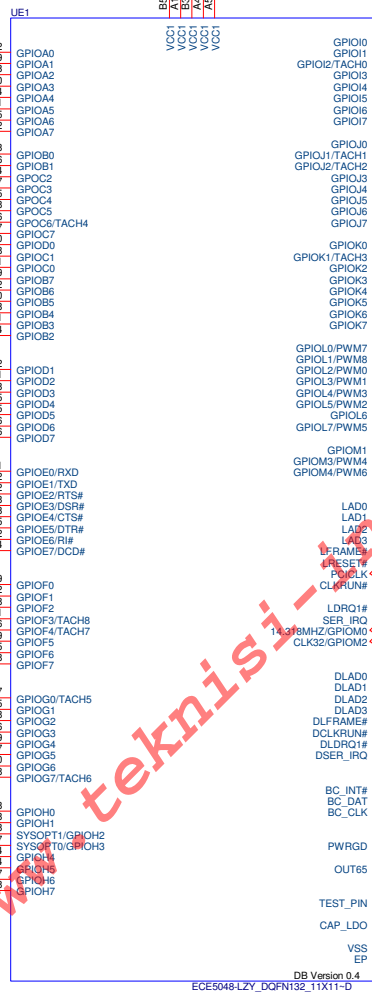
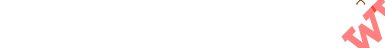
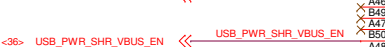
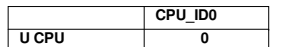
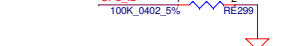
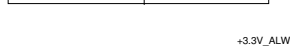
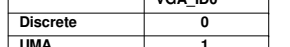
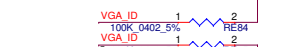
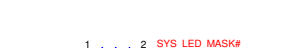
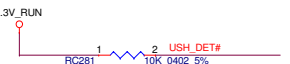
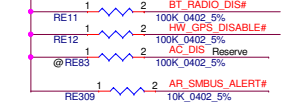
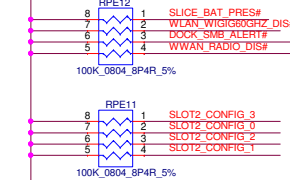
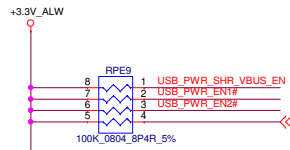
place at AGND and DGND plane

Diagram illustrating the placement of components at AGND and DGND planes. The diagram shows three parallel signal traces (RA335, RA36, RA37) connected to a common ground plane. Each trace has a 5% tolerance and a 0.0402 in length. The ground plane is labeled AGND and DGND.

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LA-C621P

Re



	VGA_ID0
Discrete	0
UMA	1

	CPU_ID0
U_CPU	0
H_CPU	1

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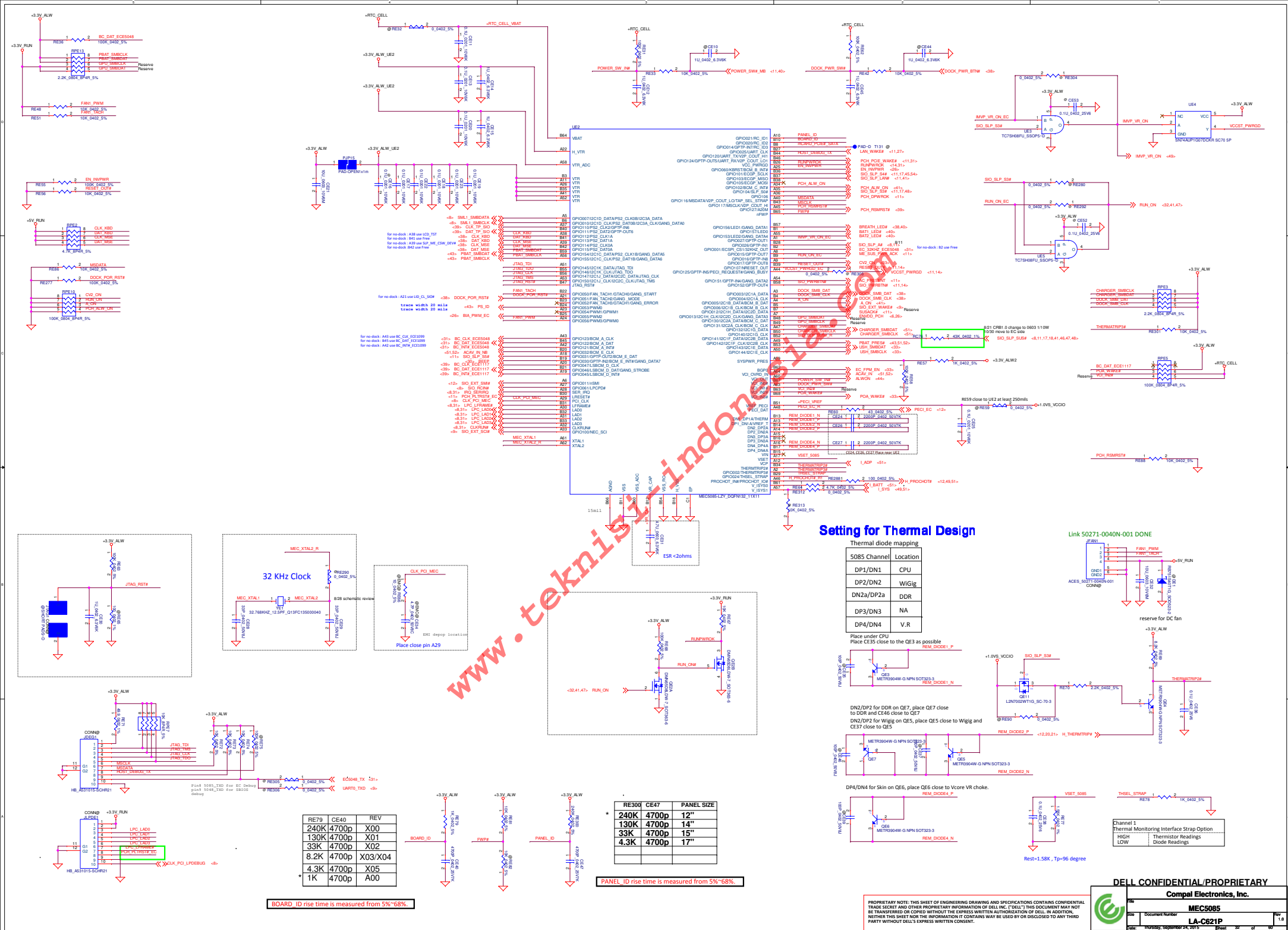
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File: **ECE5048**

Size: **LA-C621P**

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Setting for Thermal Design

5085 Channel	Location
DP1/DN1	CPU
DP2/DN2	WiGig
DN2a/DP2a	DDR
DP3/DN3	NA
DP4/DN4	V.R

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

Place under CPU
Place CE35 close to the QE3 as possible

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

PANEL ID rise time is measured from 5%-68%

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
8.2K	4700p	X03/X04
4.3K	4700p	X05
1K	4700p	A00

BOARD ID rise time is measured from 5%-68%

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MC5085

Document Number

LEC-621P

Issue

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Page

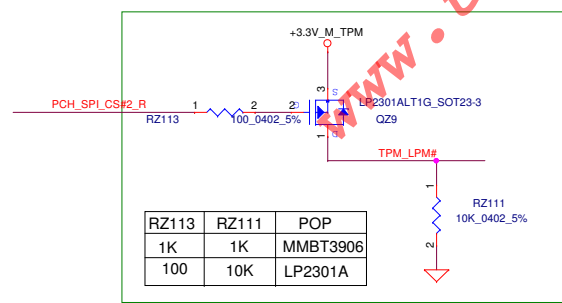
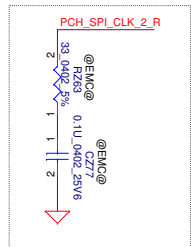
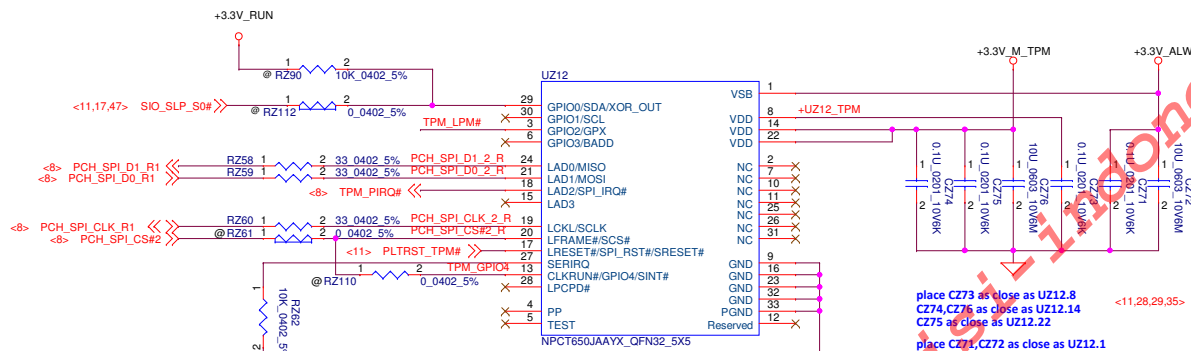
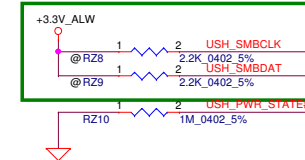
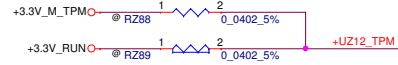
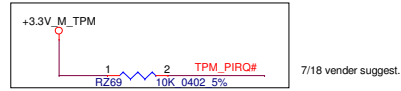
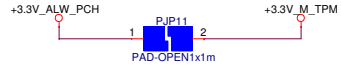
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of

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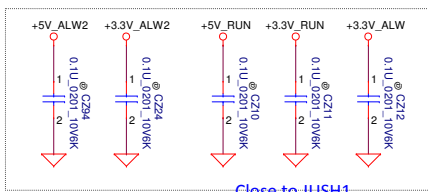
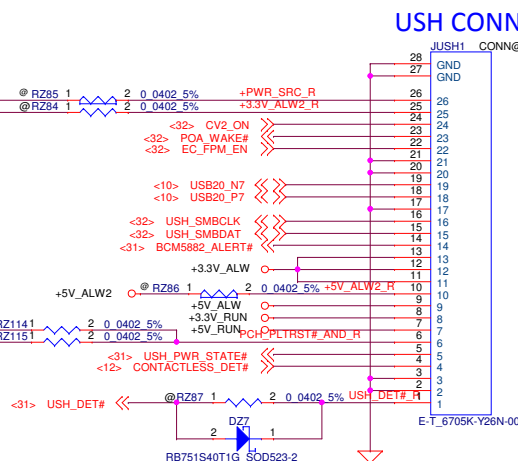
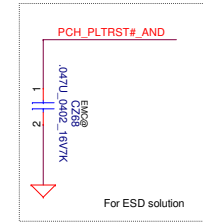
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power rail option: TPM power rail must same as +3.3V_SPI (SPI ROM)



RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A

place C273 as close as UZ12.8
C274,C275 as close as UZ12.14
C275 as close as UZ12.22
place C271,C272 as close as UZ12.1

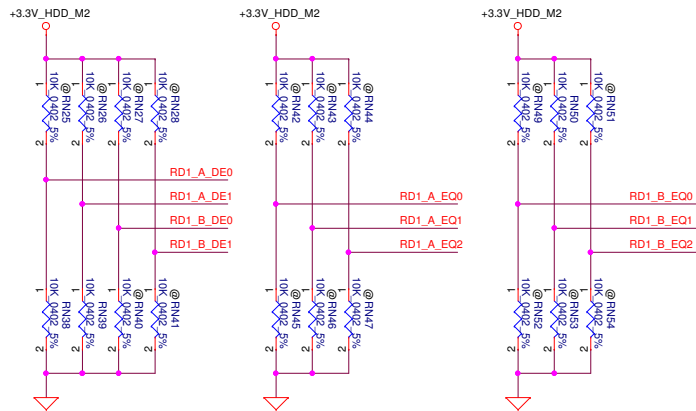


Close to JUSH1

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USH & TPM		
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Programmable output de-emphasis level setting for channel A.
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
LL: -7.5dB
HL: -2dB
LH: -3.5dB (default)
HH: -6dB

Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

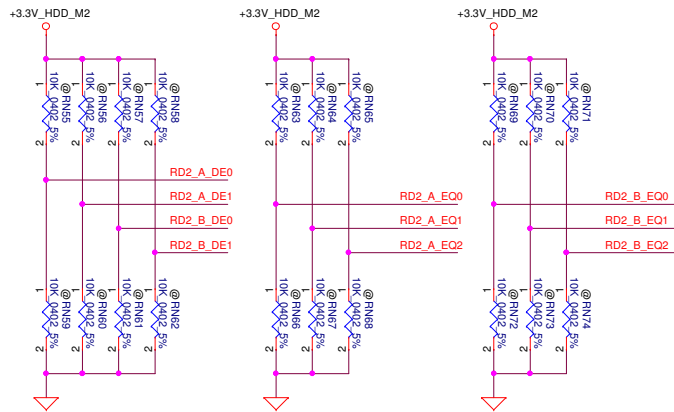
[B_DE1,B_DE0] ==
LL: -7.5dB
HL: -2dB
LH: -3.5dB (default)
HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

[A_EQ2,A_EQ1,A_EQ0] ==
LLL: EQ Level1(default)
LHL: EQ Level2
LHL: EQ Level3
HLL: EQ Level4
LHL: EQ Level5
LHH: EQ Level6
LHL: EQ Level7
HHH: EQ Level8

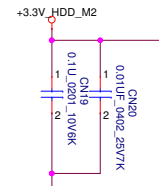
Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

[B_EQ2,B_EQ1,B_EQ0] ==
LLL: EQ Level1(default)
LHL: EQ Level2
HLL: EQ Level3
HLL: EQ Level4
LHL: EQ Level5
LHH: EQ Level6
LHL: EQ Level7
HHH: EQ Level8

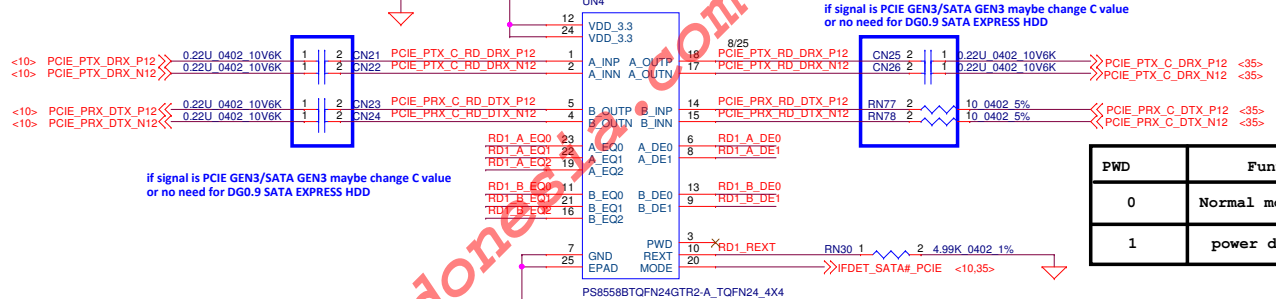


SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

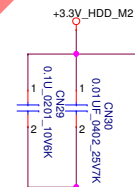


PCIE/SATA Repeater

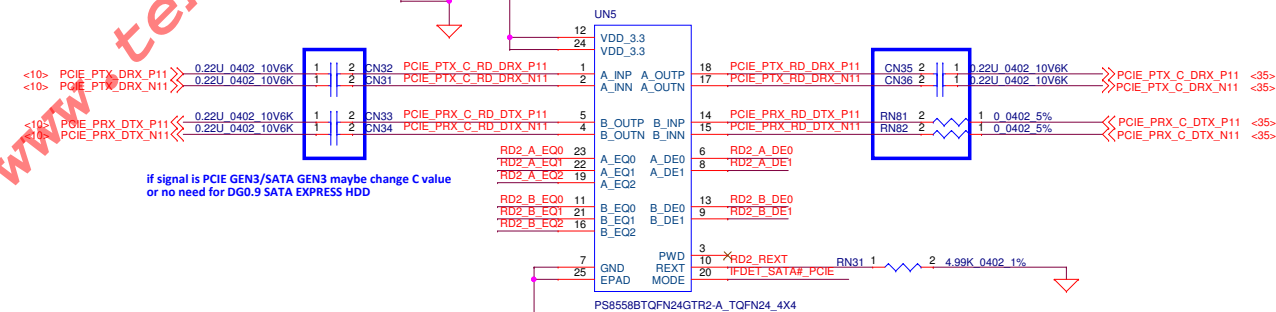


IFDET_SATA#_PCIE (SATA#PCIE0)	FLEX IO 11
0	PCIE
1	SATA

PWD	Funtion
0	Normal mode (default)
1	power down mode



PCIE/SATA Repeater

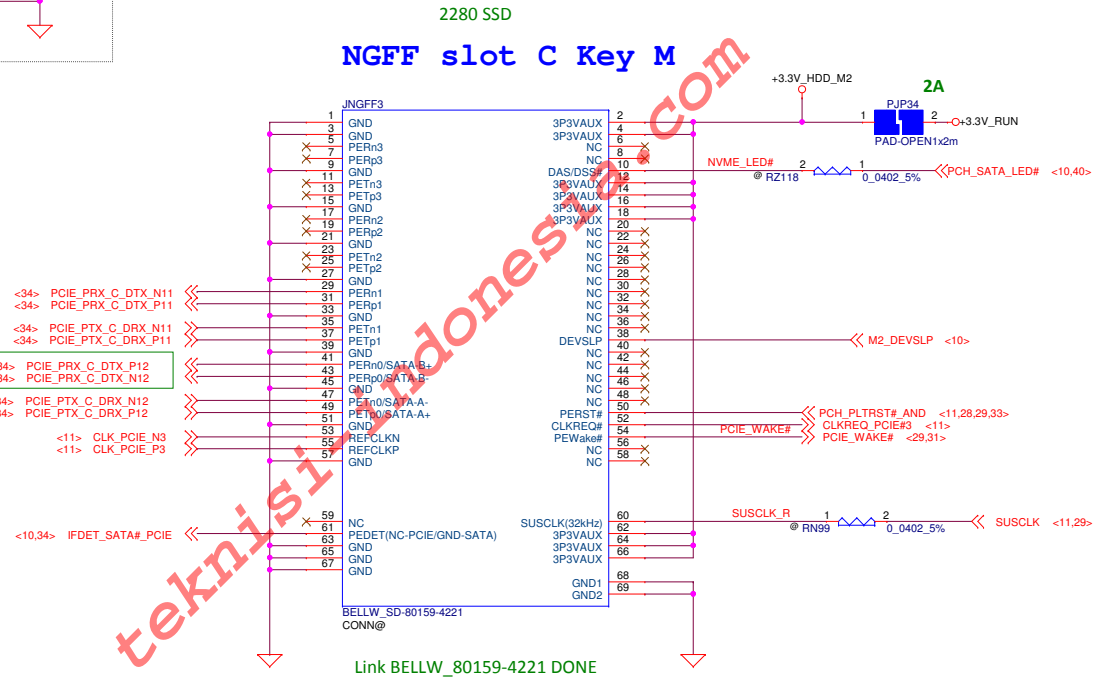
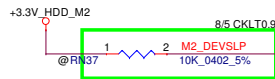
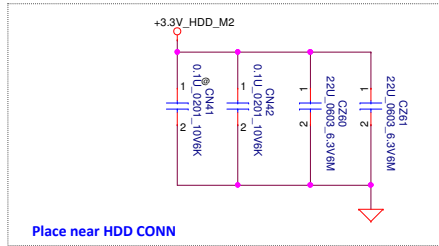


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Mini Card-2/2			
LA-C621P			
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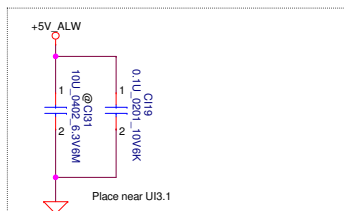
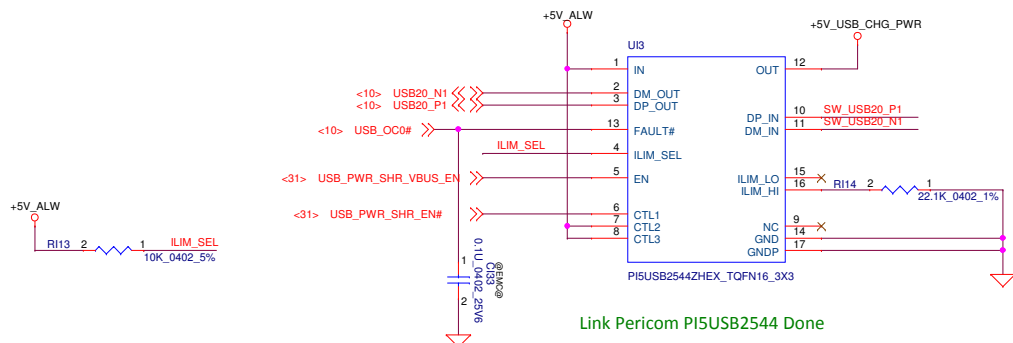
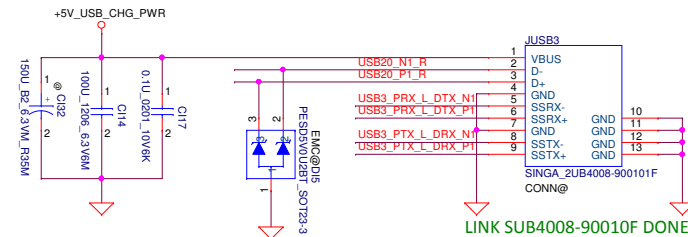
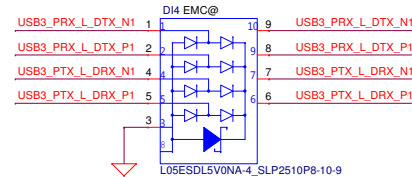
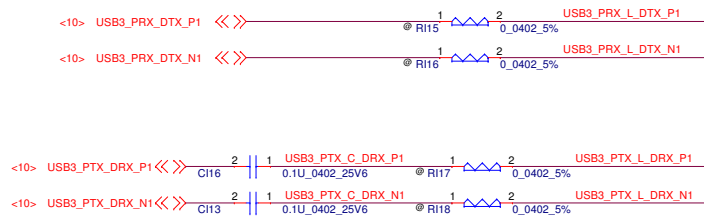
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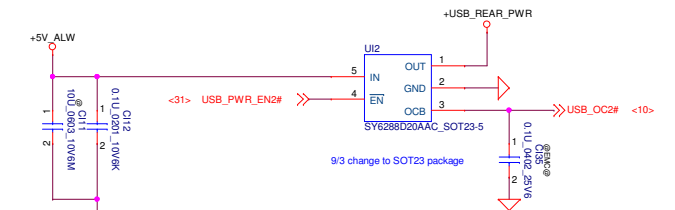
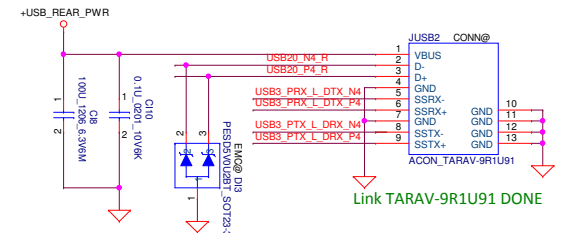
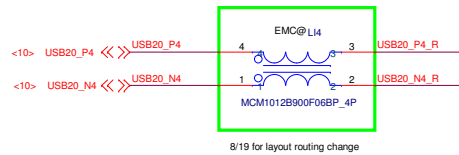
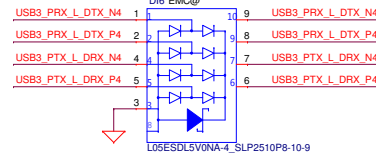
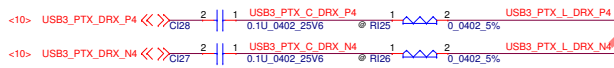
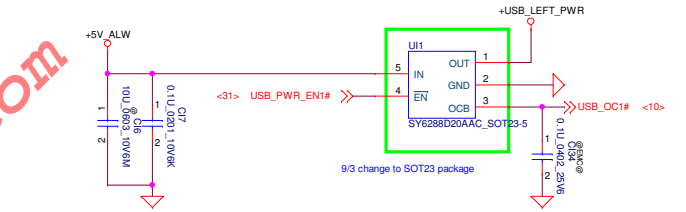
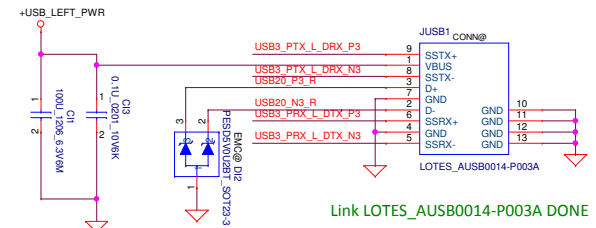
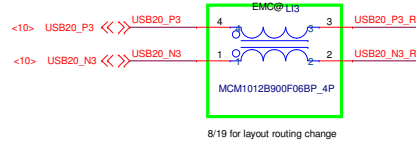
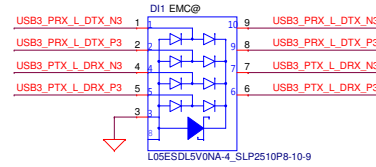
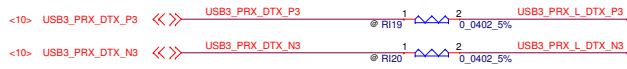
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Title		
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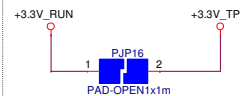
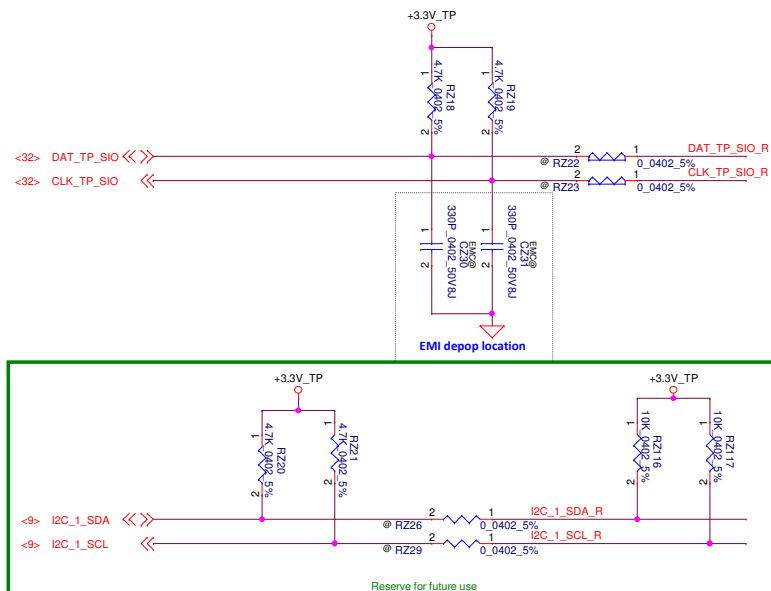
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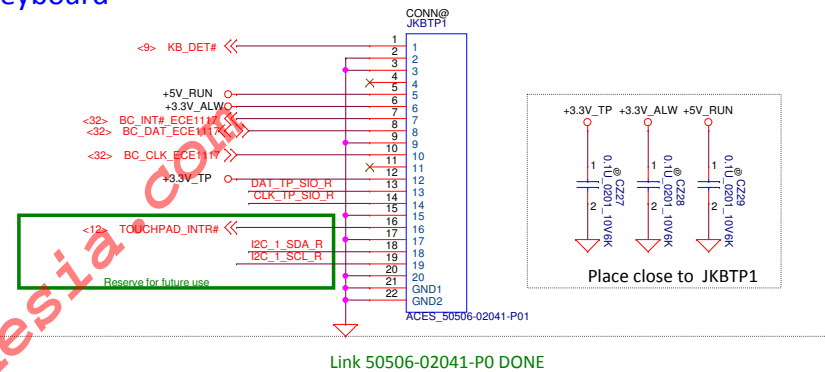
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Size	Document Number	LA-C621P	Rev 1.0
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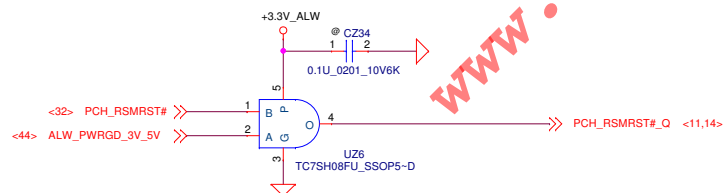
Touch Pad



Keyboard



RSMRST circuit



Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

Part Number	Description
DC301000100	CONN SET 13F DCJACK-MB 2DW1003-041110F

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 1

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDI

Part Number	Description
NBX0001J100	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

Part Number	Description
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Part Number	Description
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[illegible]

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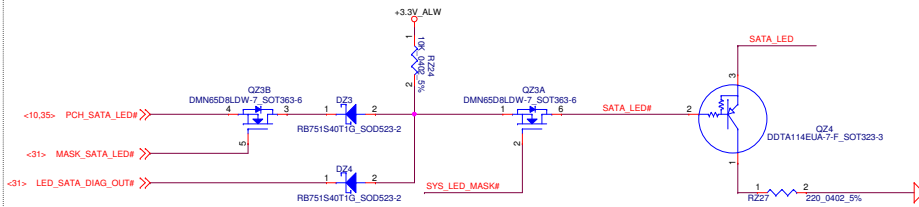
Keyboard

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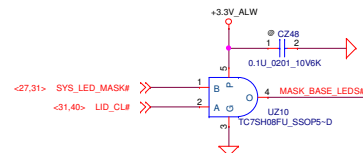
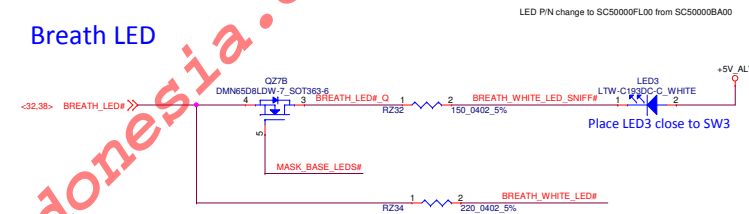
HDD LED solution for White LED



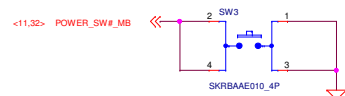
Battery LED



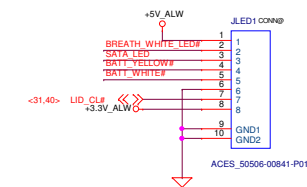
Breath LED



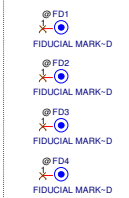
POWER & INSTANT ON SWITCH



LED board CONN

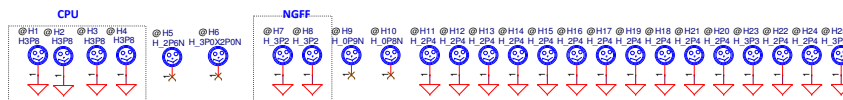


Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



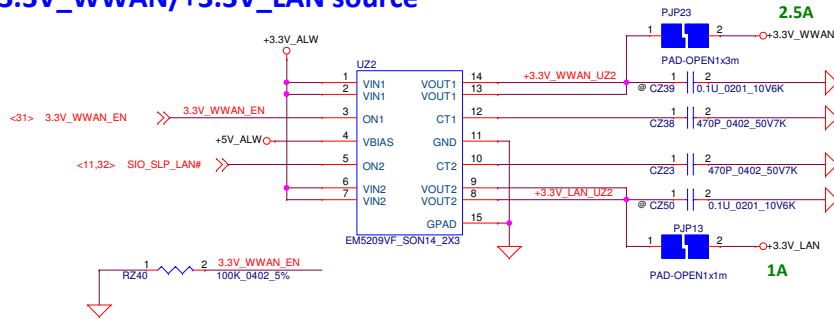
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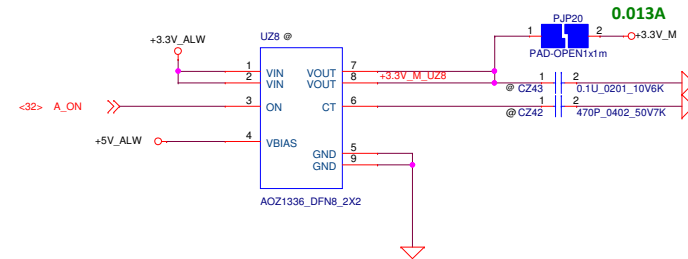
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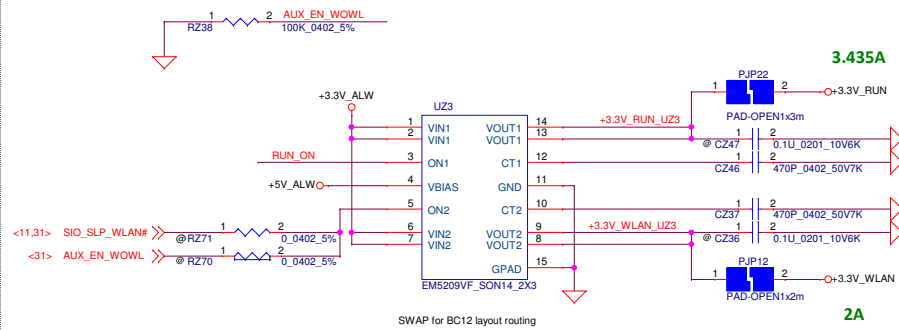
+3.3V_WWAN/+3.3V_LAN source



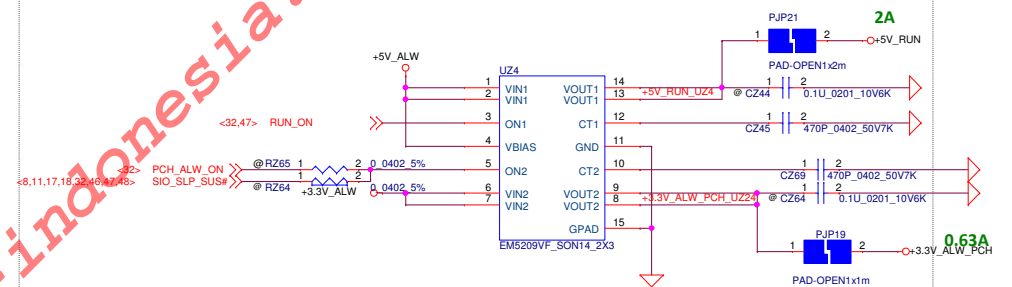
+3.3V_M source



+3.3V_WLAN/+3.3V_RUN source



+5V_RUN/+3.3V_ALW_PCH source



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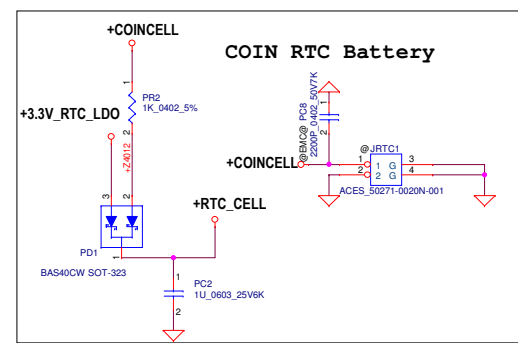
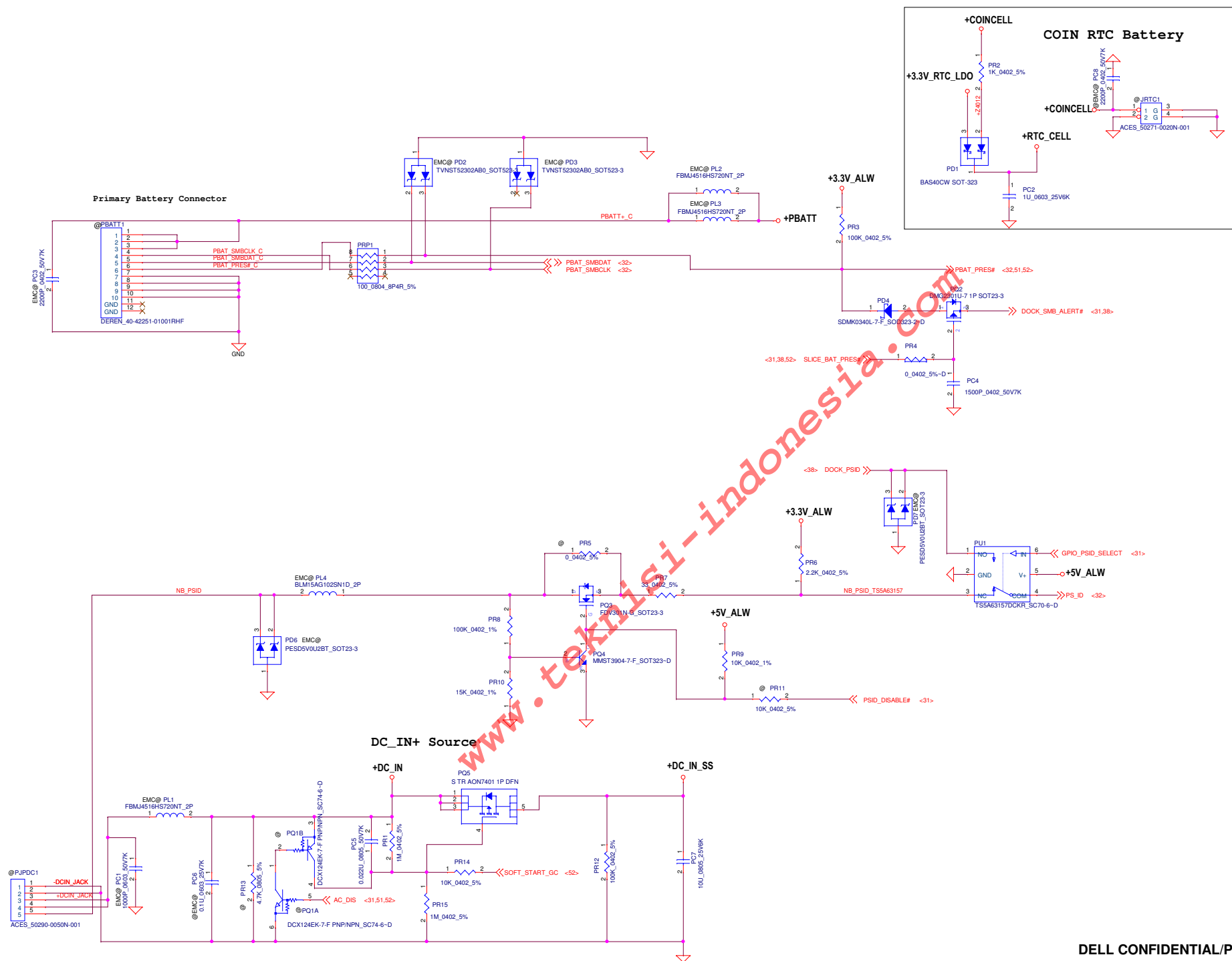
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Power control


LA-C621P

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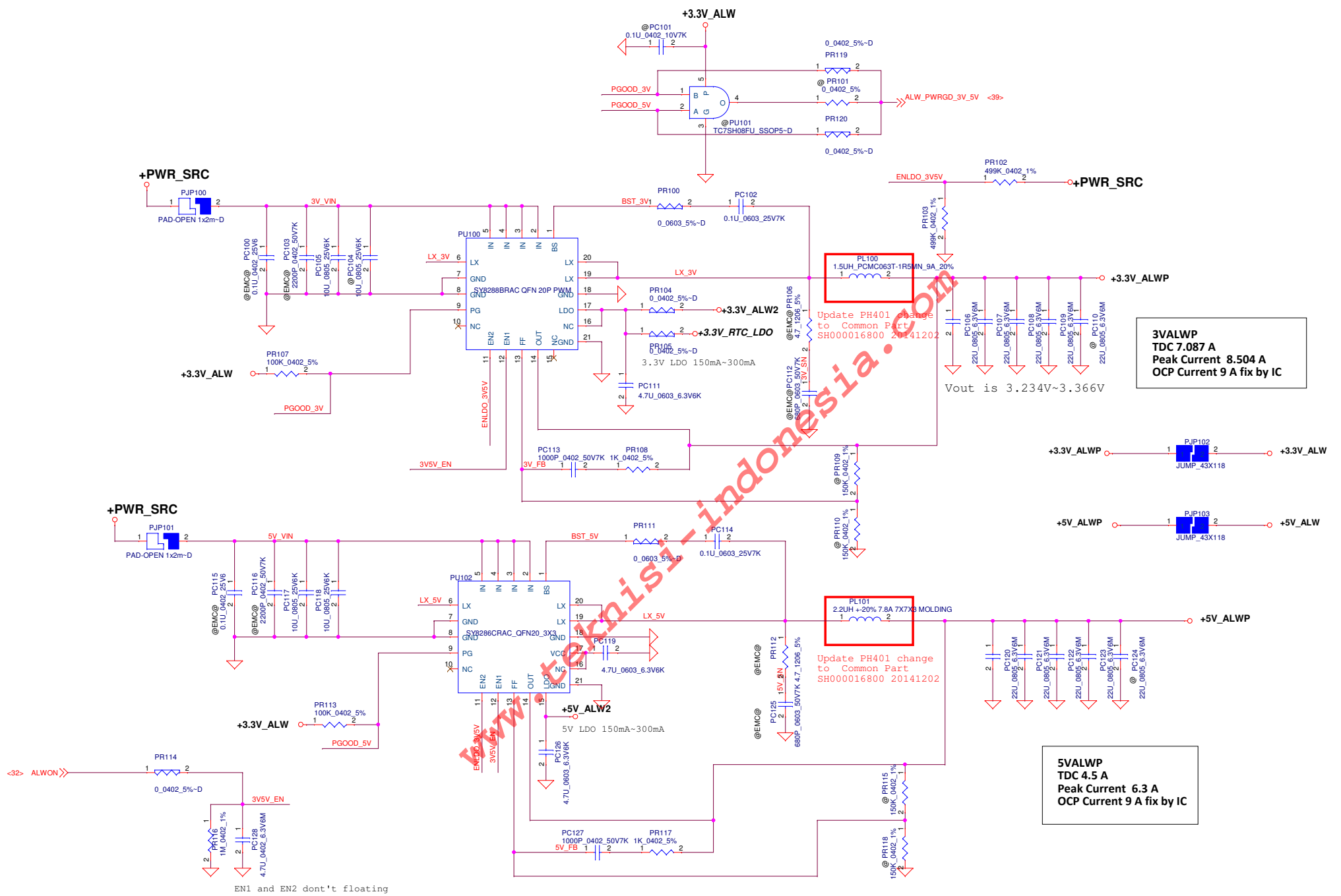
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		+DCIN	
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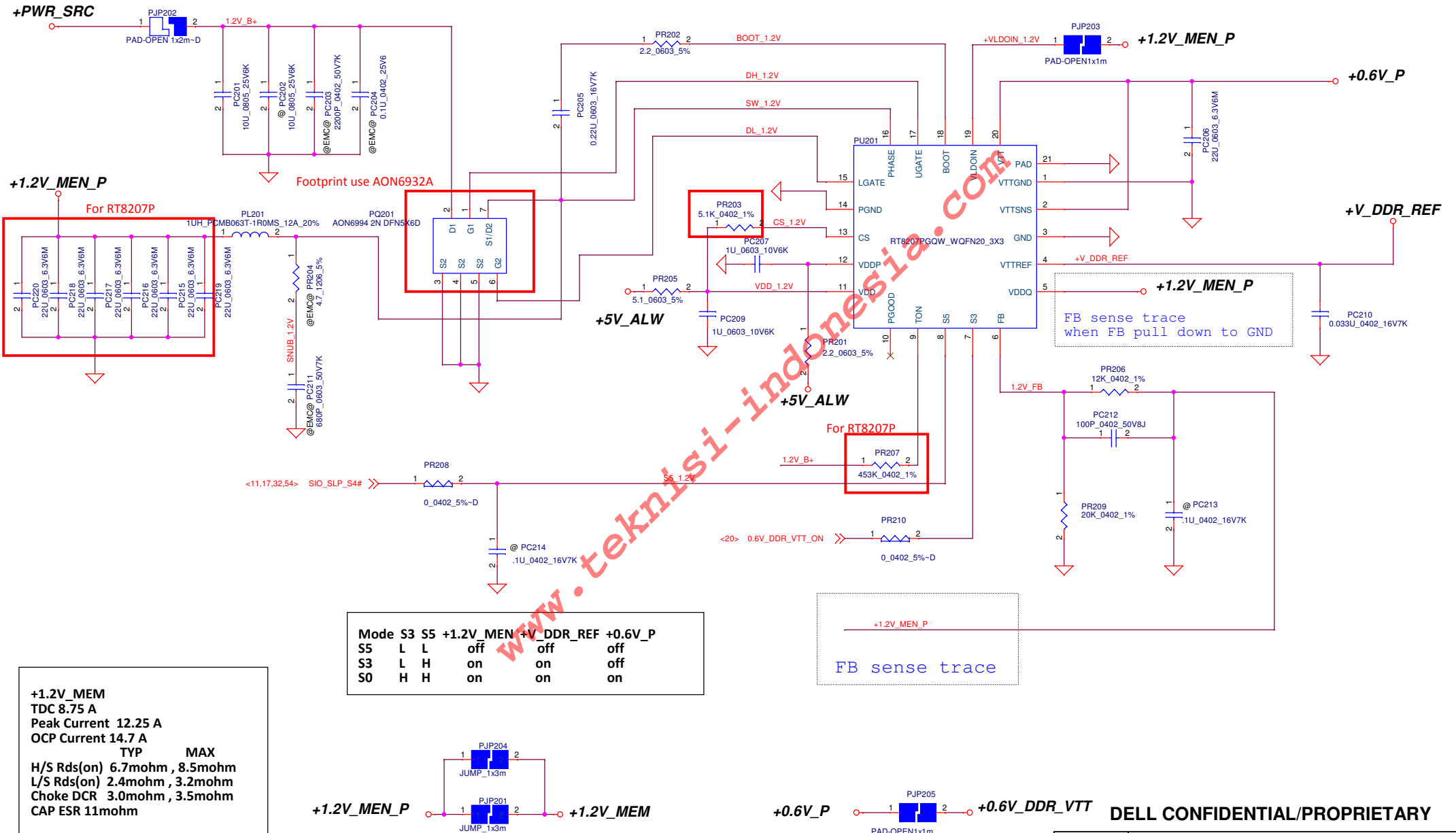


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Title			
+5V_ALW/3.3V_ALW			
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0.6Volt +/- 5%
TDC 0.7 A
Peak Current 1.0 A
OCP Current 2.6 A fix by IC



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Title
+1.2V_MEN/+0.6V_DDR VTT

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Local sense put on HW site

+1.0V_VCCST

VCC_SA
TDC 3.7A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm

VCCSA_B+
CPU_B+

VCCSA_B+

+5V_RUN

+VCC_SA

+5V_ALW

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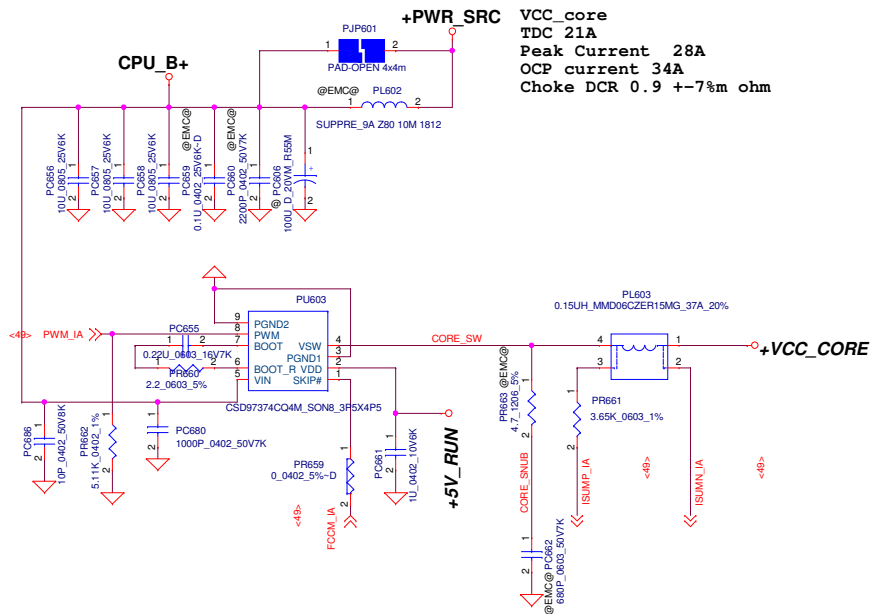
Compal Electronics, Inc.

PWR_VCORE_ISL95812 for QC

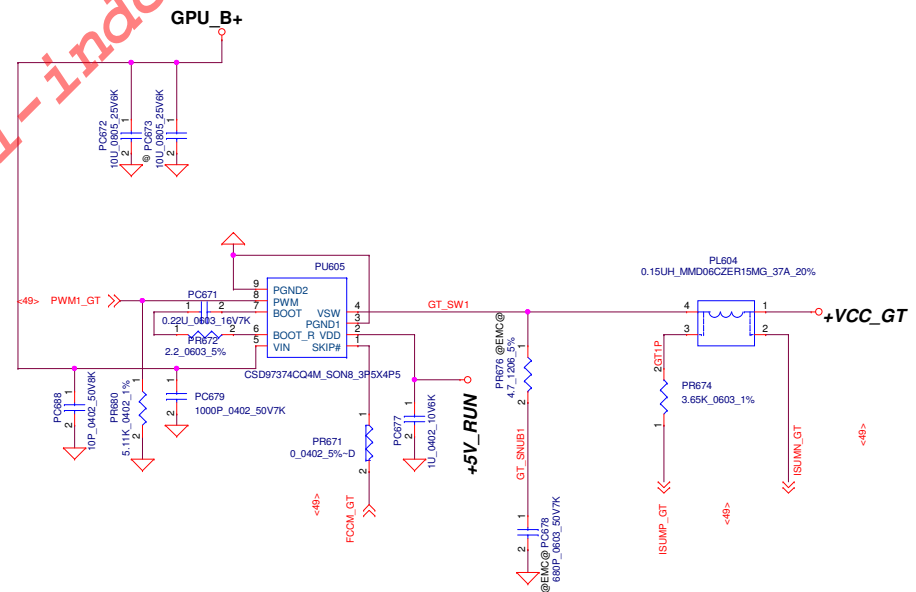
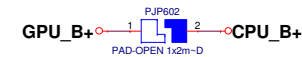
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VCC_GT
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.9 +-7% ohm



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Compal Electronics, Inc.

PWR_VCORE_ISL95812 for QC

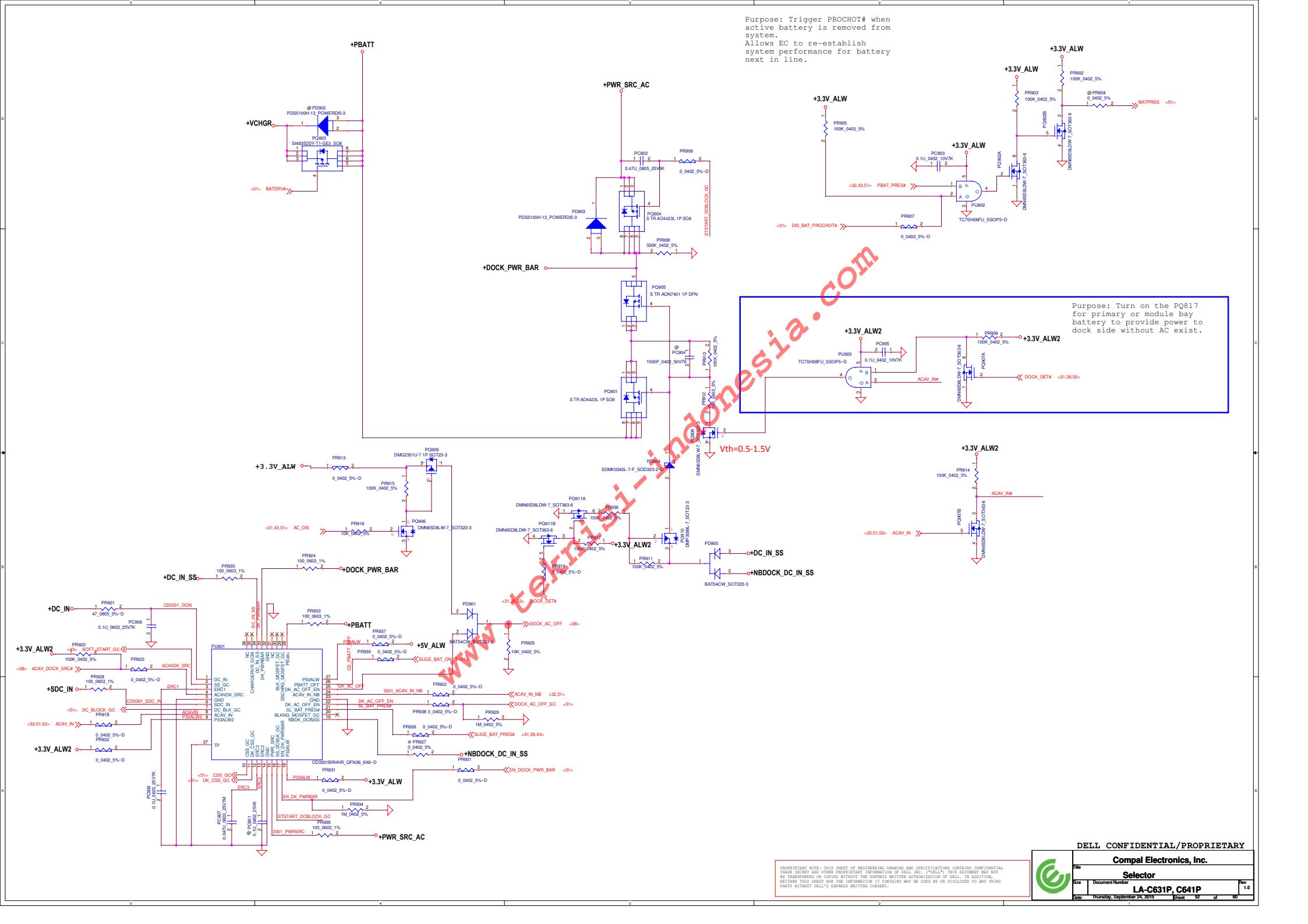
Size Document Number LA-C631P, C641P

Rev 1.0

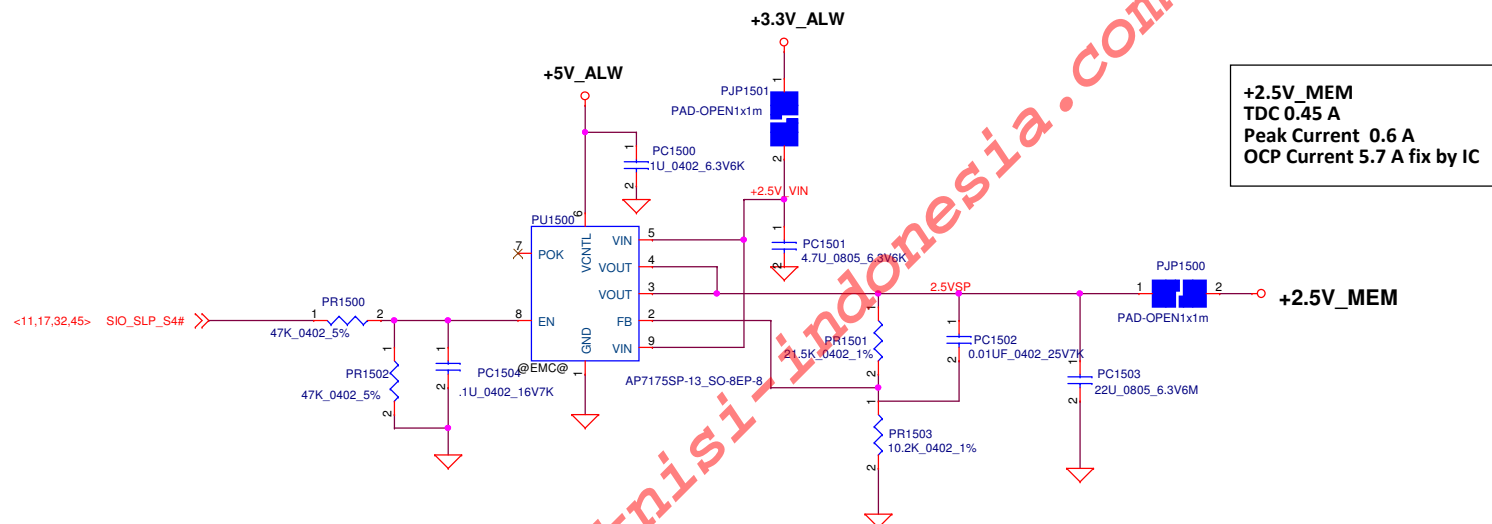
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Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.



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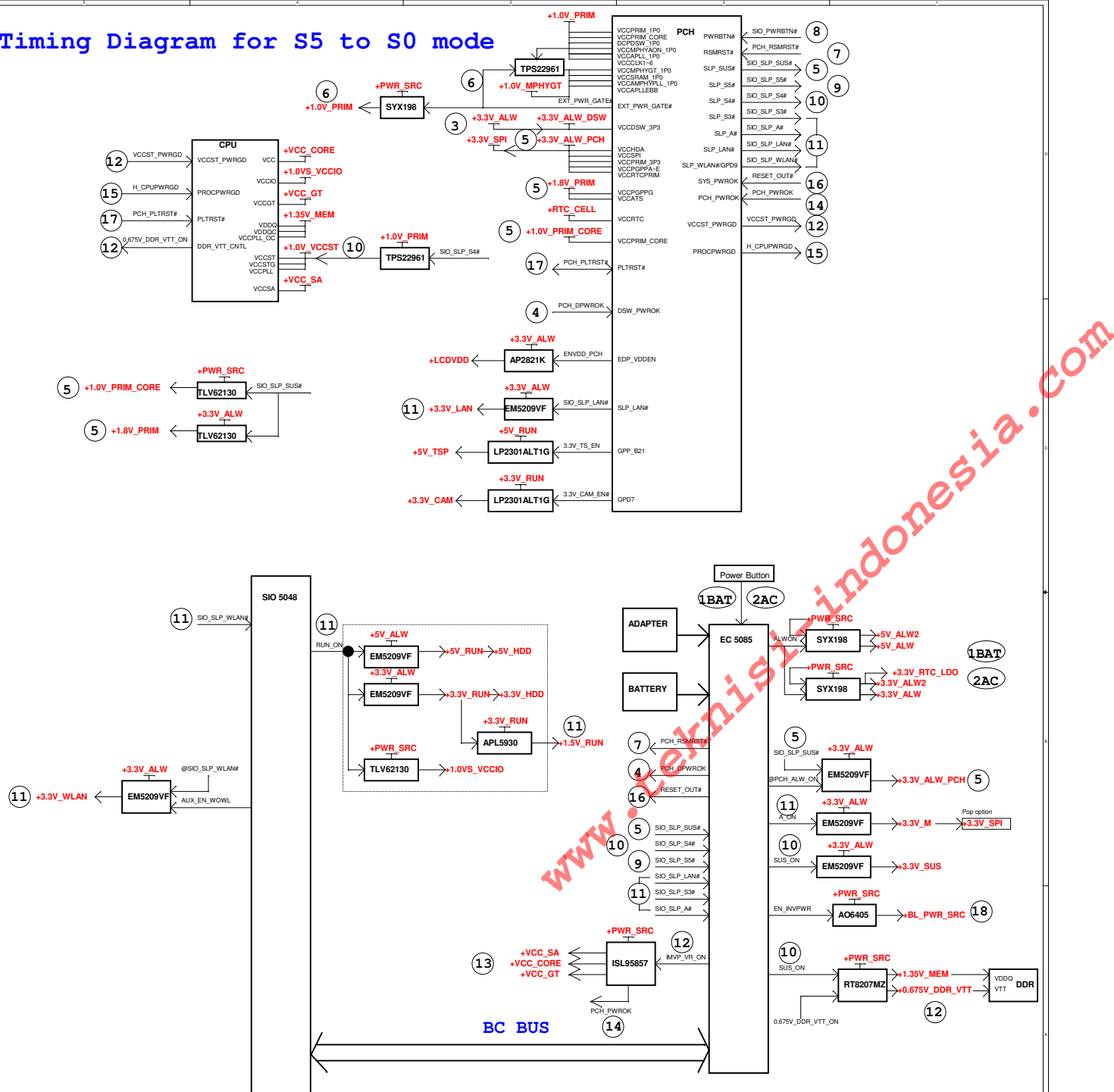


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Timing Diagram for S5 to S0 mode



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	VCCIO PRIM_COREP	1/27	Compal	For +1.0VS_VCCIO, +1.0V_PRIM_CORE IC 2nd source	Add PR403, PR406, PR427, PR428	
2	49	+VCC_CORE +VCC_SA +VCC_GT	1/27	Compal	Fine tune IMON	change PR613 to 86.6k change PR651 to 124k change PR629 to 88.7k	
3	49	+VCC_CORE +VCC_SA +VCC_GT	1/27	Compal	Fine tune VR current loop	change PR638 to 374 change PC624 to 0.033uF change PC642 to 0.1uF depop PC646	
4	44	+5V_ALW +3.3V_ALW	1/27	Compal	For 3V5V Pgood	Remove PU101, PR101, PC101 Add PR119, PR120	
5	45	+1.35V_MEM +2.5V_MEM GPU_VRAM	3/3	Compal	For DDR change to DDR3L	Remove +2.5V_MEM, GPU_VRAM power rail circuit change power setting from +1.2 to +1.35	
6	49	+VCC_CORE +VCC_SA +VCC_GT	3/27	Compal	Fine tune VR control loop	change PR640 to 340 change PC642 to 0.033uF change PC646 to 0.047uF change PR657 to 4.42k change PR628 to 4.42k	
7	45	+1.2V_MEM +2.5V_MEM GPU_VRAM	4/10	Compal	For DDR change to DDR4	Add +2.5V_MEM, GPU_VRAM power rail circuit change power setting from +1.35 to +1.2	
8	54	+2.5V_MEM +1.8VALWP +1.5VSP	4/20	Compal	Disable LDO pull up when floating enable pin	change PR1500, PR1502, PR509, PR511 to 47k	
9	51	Charger	4/20	Compal	fine tune monitor Psys	change PR822 to 40.2k	
10		+1VS_VCCIO +1.0V_PRIM_COREP				change to SY80657	
11		CPU MLCC cap cost down			CPU MLCC cap cost down	depop +VCC_CORE, 22U*15, 330U*1 +VCC_GT, 22U*8	

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
1	8/22/27/30/40/42	Material	2015/01/05	COMPAL	Material EOL	QA2, QA3, QC2, QE2, QL1, QL2, QN1, QV3, QZ3 and QZ7 from SB00000DH00 change to SB00000ZU00	0.2 (X01)
2	32	MEC5085	2015/01/05	DELL	For Next Gen EC debug	Add Re305 and RE306 reserve UART0_TXD path	0.2 (X01)
3	33	USH & TPM	2015/01/12	COMPAL	system will shut down when insert FP.	change USH conn pin define, and add RZ85, RZ86, DZ7, reserve RZ84, RZ87	0.2 (X01)
4	32	MEC5085	2015/01/12	COMPAL	change BID to X01.	change RE79 to 130K ohm.	0.2 (X01)
5	9	CPU (4/14)	2015/01/12	COMPAL	add UART port 2 for USB debug.	add net name "LPSS_UART2_TXD", "LPSS_UART2_RXD", and add RC330, RC331 and JUART1 CON	0.2 (X01)
6	13	CPU (8/14)	2015/01/12	INTEL	Follow 546765_546765_2014WW52_Skylake_MOW_Rev_1_0	reserve CC222 and RC313	0.2 (X01)
7	8	CPU (3/14)	2015/01/12	INTEL	support DCI.	add RC327 and reserve RC326, QC3	0.2 (X01)
8	32	MEC5085	2015/01/12	COMPAL	For Power down sequence.	add UE3, UE4, RE304, RE308.	0.2 (X01)
9	11	CPU (6/14)	2015/01/12	COMPAL	For PLTRST glitch issue.	1. UC7.5 change from +3.3V_RUN to +3.3V_ALW_PCH 2. Pop RC325, depop RC60.	0.2 (X01)
10	21	DDR4	2015/01/12	COMPAL	DIMM select error cause can't recognize DIMM2.	Stuff RD70, RD72 and no stuff RD69, RD73.	0.2 (X01)
11	27	Transformer	2015/01/12	COMPAL	ME height limit	TL1 changed from SP050006F00 to SP050006Y00	0.2 (X01)
12	11	Crystal	2015/01/12	TXC	Material EOS	YC2 changed from SJ10000LD00 to SJ10000LV00	0.2 (X01)
13	22	HDMI CONN	2015/01/20	COMPAL	For HDMI EMI solution.	add RV647 ~ RV658 path and depop commom-chock	0.2 (X01)
14	26	LCD	2015/01/20	COMPAL	BOM changed	UV24 from SA00006EE00 to SA00006Y800	0.2 (X01)
15	32	EC	2015/01/20	COMPAL	BOM changed	QE3/QE4/QE5/QE6/QE7 from SB000008P00 to SB000013V00	0.2 (X01)
16	32	EC	2015/01/20	COMPAL	BOM changed	UD1 and UE4 from SA00005U600 to SA00007UR00	0.2 (X01)
17	33	TPM	2015/01/20	COMPAL	TPM issue	1. Reserve 10K ohm (RZ90) and Pull-up to +3.3V_RUN on UZ12 pin 29. 2. change VSB power (UZ12.1) to +3.3V_ALW_PCH. 3. added QZ8 and RZ109 between pin3/pin20 to control LPM 4. reserve RZ110 and de-pop. 5. Reserve +3.3V_RUN on UZ12 pin 8 (add RZ88, RZ89) 6. change RZ109 pin 1 to +3.3V_M_TPM add QZ9, RZ111	0.2 (X01)
18	9	CPU (4/14)	2015/01/20	COMPAL	Non-Dock config	Reserve RH359 pull-down for non-dock config	0.2 (X01)
19	32	EC	2015/01/20	COMPAL	Power sequence fail	Depop RE280 and RE304 then pop RE292 and UE3	0.2 (X01)
20	18	CPU (13/14)	2015/02/04	COMPAL	KB boss and stand off interference	Removed RC304/RC305/RC306/CC205/CC207/CC265	0.3 (X02)
21	10	CPU (5/14)	2015/02/04	INTEL	MOW update	Add RC337 connect to GND and RC338 1K pull down	0.3 (X02)
22	12	CPU (7/14)	2015/02/04	INTEL	MOW update	Add RC328 XDP_JTAGX need connect to CPU_XDP_TCLK for DCI	0.3 (X02)
23	8	CPU (3/14)	2015/02/04	INTEL	MOW update	Changed RC317 from 4.7k to 150k and reserved SIO_SLP_SUS# on RC340	0.3 (X02)
24	20, 21	DDR4	2015/02/04	INTEL	Follow 546765_546765_2015WW02_Skylake_MOW_Rev_1_0	No stuff CD6, CD35.	0.3 (X02)

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Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
25	33	USH & TPM	2015/03/02	Nuvoton	1.for allow further reducing power in TPM 2.0 F/W,when system is in S3/4/5 and main power is off. 2.for support modern standby.	1.reserve RZ90 2.reserve RZ112. 3.Depop RZ88 and pop RZ89, pop RZ112	0.3 (X02)
26	11,27	CPU (6/14)	2015/03/02	COMPAL	Solve auto power on issue.	De-pop RL70 and pop RC323.	0.3 (X02)
27	32	MEC5085	2015/03/02	COMPAL	Solve power down sequence fail.	De-pop RE308.	0.3 (X02)
28	32	MEC5085	2015/03/02	COMPAL	change BID to X02.	change RE79 to 33K ohm.	0.3 (X02)
29	26	eDP CONN & TS	2015/03/02	DELL	Customer request.	add 6 pin IR Conn.	0.3 (X02)
30	40	PAD, LED	2015/03/02	COMPAL	ME design change.	change H6 from 4mm to 3mm.	0.3 (X02)
31	11/32	Crystal	2015/03/02	COMPAL	X'tal EA measurement.	change CC23 and CC26 from 18pf to 12pf	0.3 (X02)
32	8	CPU (3/14)	2015/03/02	Intel	Intel MOW_2015WW06:Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update	de-pop RC30, RC316	0.3 (X02)
33	8	CPU (3/14)	2015/03/02	COMPAL	Follow CRB setting	RC23 changed from 8.2K to 2.2K	0.3 (X02)
34	33	TPM	2015/03/02	COMPAL	support modern standby	Add RZ112 connect to SIO_SLP_S0# with TPM	0.3 (X02)
35	32	EC	2015/03/02	COMPAL	Option DDR3L and DDR4	Add GPP_D9(DIMM_TYPE), RC342 and RC341 that selected DDR3L and DDR4.	0.3 (X02)
36	32	EC	2015/03/02	COMPAL	Follow Intel power sequence	Pop RE292 and depop RE280	0.3 (X02)
37	8	CPU (3/14)	2015/03/02	COMPAL	RF request	Pop CC3/CC4/CC5/CC6 from 22p to 27p	0.3 (X02)
38	33	TPM	2015/03/02	Nunoton	TPM detected sequence	Add RZ113 100 ohm	0.3 (X02)
39	11	CPU (6/14)	2015/03/02	COMPAL	Deep S3 leakage	VRLERT# changed power rail from +3.3V_ALW to +3.3V_ALW_PCH	0.3 (X02)
40	27	LAN	2015/03/02	COMPAL	IEEE EA measurement.	change LL2 ~ LL9 to 2.2 ohm Res (RL71~RL78).	0.3 (X02)
41	9	CPU (4/14)	2015/04/02	COMPAL	IR Function	1.add IR_CAM_DET# on JIR1 pin 1. 2.add IR_CAM_DET# on UCL.AW7, and PU 100K(RC346) to +3.3V_RUN	0.4 (X03)
42	31/33	EC/USH	2015/04/02	Broadcom	Vender recommend	1.Reserve RZ114/RZ115 on JUSH1 pin 21 2.add USH_RST# on UE1.A62	0.4 (X03)
43	12	CPU (7/14)	2015/04/02	COMPAL	SIO_EXT_SMI# to wake up system when non-deep S3	Add RC236 SIO_EXT_SMI# change power to +3.3V_ALWS_PCH	0.4 (X03)
44	29	NGFF Card	2015/04/02	COMPAL	ME request	Change JSIM1 conn to T-SOL_5-991503004000-6	0.4 (X03)
45	32	MEC5085	2015/04/02	COMPAL	change BID to X03	change RE79 to 1K ohm.	0.4 (X03)
46	9	CPU (4/14)	2015/04/02	COMPAL	for DIMM type option	Pop RC342 and de-pop RC341	0.4 (X03)
47	40	PAD, LED	2015/04/02	COMPAL	ME request	Add H9 and H10 for different SIM CON	0.4 (X03)
48	29	NGFF	2015/04/02	COMPAL	SIM detect	Add RI31 connecting with JSIM1.9 and NGFF2.58	0.4 (X03)
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Version Change List (P. I. R. List)

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49	39	KB	2015/04/20	ALPS	For new U1 TP module	Add RZ116 and RZ117 PU on I2C._1_SDA_R/I2C_1_SCL_R	0.4 (X03)
50	31	5048	2015/04/20	COMPAL	PC common EC code issue need reserved PU	Add AR_SMBUS_ALERT# 10K(RE309) PU on ECE5048 pin58 GPIOF2	0.4 (X03)
51	31	All	2015/04/20	COMPAL	Changed 0 ohm short-pad	R274, RA35, RA36, RA37, RC143, RC169, RC170, RC171, RC172, RC173, RC211, RC214, RC228, RC229, RC230, RC231, RC235, RC290, RC295, RC296, RC299, RC300, RC301, RC302, RC303, RC307, RC308, RC309, RC310, RC325, RC327, RC328, RC337, RC37, RD29, RD60, RD65, RD66, RD67, RD68, RD70, RD72, RD74, RE290, RE305, RI15, RI16, RI17, RI18, RI19, RI20, RI21, RI22, RI23, RI24, RI25, RI26, RI27, RI28, RI29, RI30, RI31, RL34, RL7, RN99, RR17, RR18, RR21, RR22, RR23, RZ22, RZ23, RZ56, RZ70, RZ85, RZ86	0.4 (X03)
52	8	CPU(3/14)	2015/04/20	COMPAL	SMBUS LAN backdrive	Add RC347 and RC348 PU to +3.3V_ALW_PCH	0.4 (X03)
53	11	CPU(6/14)	2015/05/20	COMPAL	Crystal EA -R issue	Changed YC2-CL 9pf from 12pf and cc23/cc26 changed to 6pf from 12pf	0.5 (X04)
54	35	M2280	2015/05/20	COMPAL	Insert NVME SATA LED no function	JNGFF3.10 connected to PCH_SATA_LED#	0.5 (X04)
55	36	USB	2015/05/20	COMPAL	Insert Storage Bus shutdown	Add CI32 150U prevent charger current over spec	0.5 (X04)
56	39	TP	2015/05/20	COMPAL	TP function sometimes lag or crazy	CZ30 and CZ31 change from 10p to 330p improve signal quality	0.5 (X04)
57	31	5048	2015/05/20	COMPAL	For Type-C function	1. Add 5048 GPIO(PROCHOT_GATE) and reserve RE311 pull high 2. Add 5048(PD_ACE_DET#) for AR config and pull high on RE310	0.5 (X04)
58	32	MEC5085	2015/05/20	COMPAL	change BID to X04	change RE79 to 8.2K ohm.	0.5 (X04)
59	18	CPU(13/14)	2015/05/27	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	1.Add RC349 and CC303 on VCCHDA 2.Add RC350 and CC304 on VCCAPLL_1P0	0.5 (X04)
60	36/37	USB3.0	2015/05/27	COMPAL	ESD request	1.Add CI33 0.1U cap to GND on USB_OC0# 2.Add CI34 0.1U cap to GND on USB_OC1# 3.Add CI35 0.1U cap to GND on USB_OC2#	0.5 (X04)
61	26	eDP	2015/06/27	COMPAL	Material shortage	Changed DV1, DV2 and DV3 from SCS00003800 to SCS00006400	0.6 (X05)
62	33	TPM	2015/06/27	COMPAL	Change TPM FW to 1.2 version	Changed UZ12 from SA000082D00 to SA00008EL20	0.6 (X05)
63	32	KBC	2015/06/27	COMPAL	WinPE Global reset shutdown issue	Add QE11 prevent +1.0V_VCCST timing down before +1.0V_VCCIO	0.6 (X05)
64	32	KBC	2015/06/27	COMPAL	Follow intel power sequence	Add UE5 AND Gate control Run_on timing and depop RE292	0.6 (X05)
65	11	CPU(6/14)	2015/06/27	COMPAL	Cystal EA	Changed CC21 and CC22 from 22p to 15p	0.6 (X05)
66	33	USH	2015/06/27	COMPAL	TPM1.2 deep S3 resume issue	UZ12.1 changed power rail from +3.3V_ALW_PCH to +3.3V_ALW	0.6 (X05)
67	24	DP HUB	2015/07/20	COMPAL	For DP hub display flicker issue	1.Add UV29, CV617, CV618, CV619, RV659, RV650, RV661 2.Depop UV28, PJP33, CV615, CV616	0.6 (X05)
68	36	HW	2015/07/20	COMPAL	For Sourcer request	CI32 change from SGA00002N80 to SGA00004E10	0.6 (X05)
69	32	MEC5085	2015/07/20	COMPAL	change BID to X05	change RE79 to 4.3K ohm.	0.6 (X05)

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Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
70	41	CPU(12/14)	2015/07/31	COMPAL	Follow Intel DG1.5	Add load switch (UZ26) control to +VCCPLL_OC power rail	0.6(X05)
71	18	CPU(13/14)	2015/07/31	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	Change RC349 and RC350 to LC1 and LC2	0.6(X05)
72	36	USB	2015/08/12	COMPAL	Low battery shut down issue	Depop CI32 and then pop CI14	0.6(X05)
73	32	5085	2015/08/12	COMPAL	DC mode CPU trubo issue	Reserved RE313 pull down path on I_SYS	0.6(X05)
74	34	PCIE	2015/08/12	COMPAL	M.2 SATA iEMT	Pop RN50 change to level2	0.6(X05)
75	11	CPU(6/14)	2015/08/12	COMPAL	RTC delay	YC2 changed to 10ppm(SJ10000Q800) and CC23/CC26 changed to 5pf	0.6(X05)
76	24	HUB	2015/09/12	COMPAL	Display no function	RV662 chnanged to 0 ohm from 1 ohm.	1.0(A00)
77	ALL	All	2015/09/12	COMPAL	Changed 0 ohm short-pad	RC41,RC289,RZ89,RZ112,RZ64,RC221,RZ118,RV662	1.0(A00)
78	12	CPU(7/14)	2015/09/12	COMPAL	Service mode switch	Depop RC222 and SW1 and then short RC221	1.0(A00)
79	32	5085	2015/09/12	COMPAL	syn-up with power material issue	1.Change SC600001600 to SCA00000T00 (DI2,DI3,DI5,DV4) 2.Change SB000013V00 to SB00000Z500 (QE3,QE4,QE5,QE6,QE7)	1.0(A00)
80	32	MEC5085	2015/09/12	COMPAL	change BID to A00	change RE79 to 1K ohm.	1.0(A00)
81	22	HDMI	2015/09/18	COMPAL	DFX request	Delete LV3/LV6/LV9/LV12 co-lay footprint	1.0(A00)
82	12/14	XDP	2015/09/20	COMPAL	Follow PDG2.0	Changed RC82 and RC135 to 100 from 51.	1.0(A00)
							

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